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VK1S68C Datasheet

13×4/12×5/11×6/10×7
LED DRIVER
Rev.1.3

1 General Description

The VK1S68C is a dedicated chip for digital tube or dot matrix LED driver control with a keyboard scanning interface. It integrates a 3-wire serial interface, data latch, LED driver, keyboard scanning and other circuits internally. The SEG pin is connected to the anode of the LED, and the GRID pin is connected to the cathode of the LED. It can support dot matrix LED display panels with 13SEG×4GRID, 12SEG×5GRID, 11SEG×6GRID, and 10SEG×7GRID, with a maximum support of 10x2 keys. It is suitable for products that require reliability, stability and strong anti-interference ability.

2 Key Features

∇ Operating voltage：3.0-5.5V

- Built-in RC oscillator
- 10 SEG pins, 4 GRID pins, and 3 configurable SEG/GRID multiplexing pins
- The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED
- 10×2 matrix keys, supporting simultaneous pressing of multiple keys (Key display multiplexing requires hardware circuit coordination.)
- 3-wire serial interface
- The overall brightness is adjustable at 8 levels
- The built-in display RAM is 14×8 bits
- Built-in power-on reset circuit
- Strong anti-interference ability
- Available Packages:
  SSOP24(150mil)(8.65mm × 3.90mm PP=0.635mm)

3 Application Field

∇ Small household appliances
∇ Induction cooker/microwave oven
∇ Pressure gauge

4 Product Selection

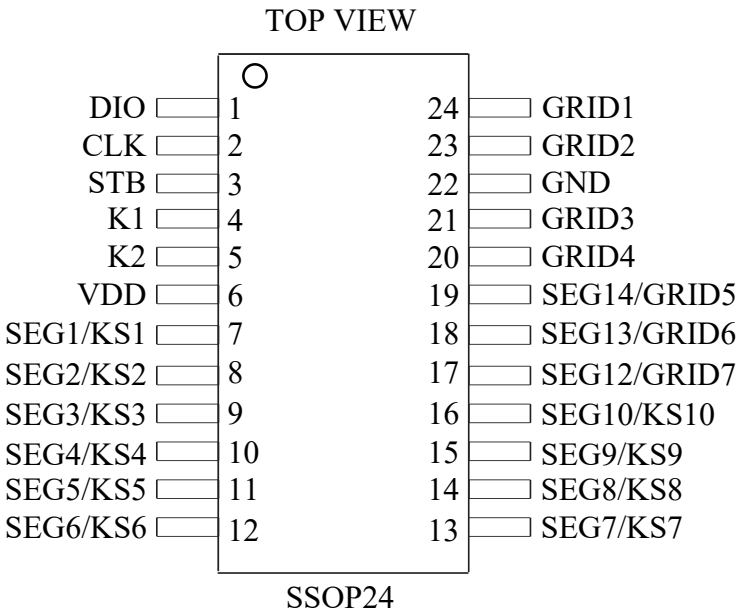
Part No.	Common Cathode Drive	Common Anode Drive	Key press	Packaging
VK1616	7 / 4	4 / 7	---	SOP16
VK1618	5 / 7 , 6 / 6 7 / 5 , 8 / 4	7 / 5 , 6 / 6 5 / 7 , 4 / 8	5×1	SOP18
VK1620	8 / 6 , 9 / 5 10 / 4	6 / 8 , 5 / 9 4 / 10	---	SOP20
VK1624	11 / 7 , 12 / 6 13 / 5 , 14 / 4	7 / 11 , 6 / 12 5 / 13 , 4 / 14	---	SOP24
VK1S68C	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	SSOP24
VK1Q68D	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	QFN24L (4mm*4mm）
VK1668	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	SOP24
VK1668B	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	SSOP24
VK1628	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	SOP28
VK1628A	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	SSOP28

Note: For both common cathode and common anode digital tubes, SEG is connected to the anode and GRID to the cathode.

5 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel) Qty	Box Qty	Total Qty	Notes
VK1616	SOP16	50/tube		10000/box	100000 PCS	
VK1618	SOP18					
VK1620	SOP20	36/tube		2880/box	28800 PCS	
VK1624	SOP24	30/tube		2400/box	24000 PCS	
VK1S68C	SSOP24	50/tube		10000/box	100000 PCS	
VK1Q68D	QFN24L (4mm*4mm)		3000/reel		24000 PCS	reel
VK1668	SOP24	30/tube		2400/box	24000 PCS	
VK1668B	SSOP24	50/tube		10000/box	100000 PCS	
VK1628	SOP28	26/tube		2080/box	20800 PCS	
VK1628A	SSOP28	50/tube		5000/box	50000 PCS	

6 Package Pinout Information(SSOP24)



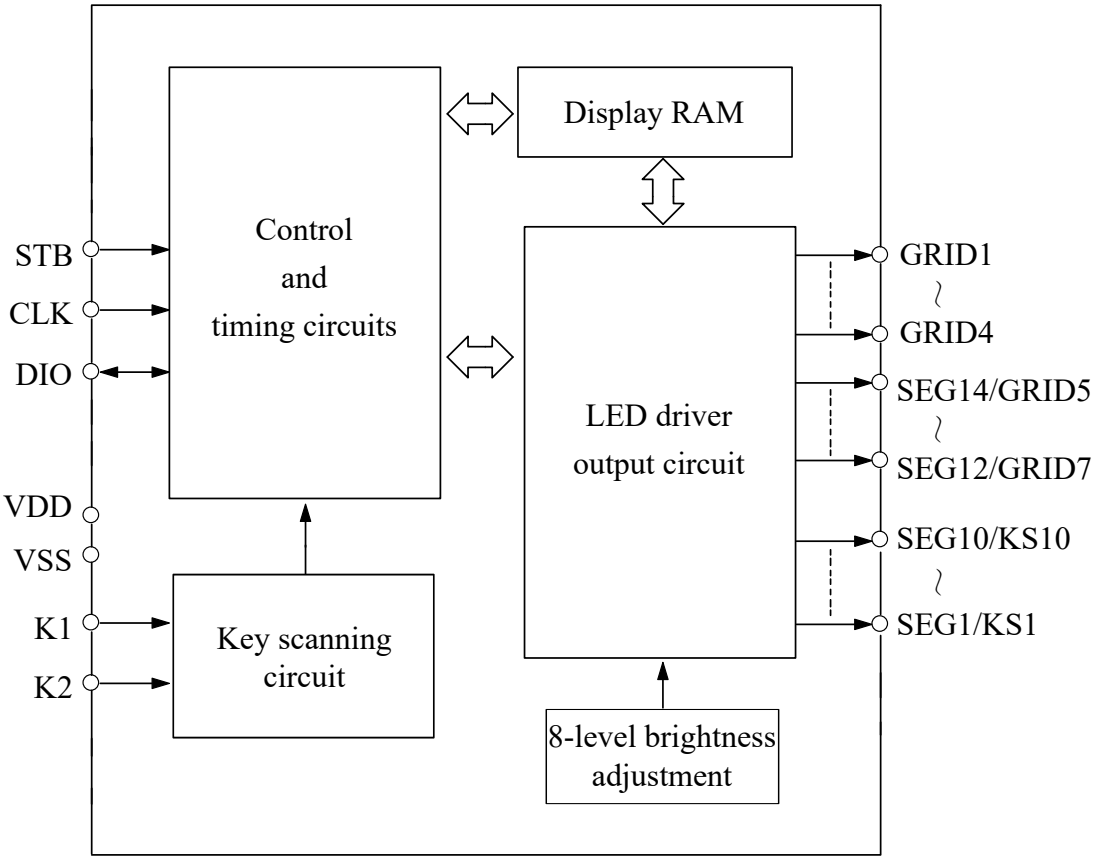
For more information: Page 19

6.1 VK1S68C/SSOP24 Pin Description

No.	Name	I/O	Function
1	DIO	I/O	Bidirectional data (NMOS open leakage), data input/output starts from the lower bit. Read the DIO pin data to the display RAM at the rising edge of the clock and output the data to the DIO pin at the falling edge of the clock.
2	CLK	I	The clock signal reads DIO pin data to the display RAM at the rising edge and outputs data to the DIO pin at the falling edge.
3	STB	I	Chip selection signal, high level disabled, low level enabled.
4，5	K1，K2	I	Key scanning input, the key signal is latched after the display cycle ends
6	VDD	VDD	Positive power supply
7-16	SEG1/KS1-SEG10/KS10	O	LED SEG output (P-channel)
17, 18, 19	SEG12GRID7-SEG14/GRID5	O	LED SEG/GRID multiplexing output can be configured as either SEG output or GRID output through software
20, 21 23,24	GRID4-GRID1	O	LED GRID output (N-channel open-drain output)
22	GND	VSS	Negative power supply

7 Functional Description

7.1 Block Diagram



7.2 Display RAM- Storage Structure

The static display memory (RAM) has a structure of 14×8 bits and stores the displayed data. The content of RAM is directly mapped to the display content of the LED driver, with the display address being 0xC0-0×CD, and there are a total of 14 display units. If you want to turn on or off a certain LED, simply set the corresponding display RAM position to 1 or clear to 0. For example, to control the on/off of LED1 driven by pins SEG1 and GRID1, simply set the bit0 position of the corresponding display RAM (address 0×C0) to 1 or clear to 0. Clear the RAM bits corresponding to the unused SEG pins in the application to 0.

The process of mapping the contents in RAM to LED is shown in the following table:

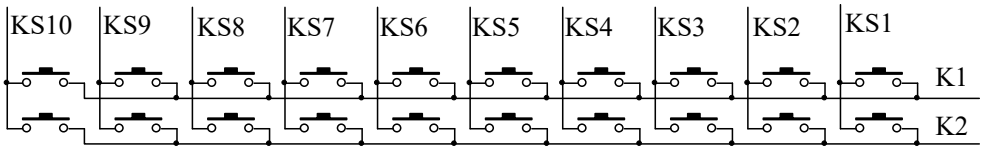
SEG / GRID	X	X	SEG14	SEG13	SEG12	X	SEG10	SEG9	Addr	SEG8	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	Addr	SEG / GRID
GRID1									0xC1								LED1	0xC0	GRID1
GRID2									0xC3									0xC2	GRID2
GRID3									0xC5									0xC4	GRID3
GRID4									0xC7									0xC6	GRID4
⋮				⋮					⋮				⋮					⋮	⋮
GRID7									0xCD									0xCC	GRID7
	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0		

Note:

1. The value stored inside the chip display RAM at the moment of power-on may be random. It is recommended that the customer perform a power-on reset of the display RAM, that is, write all the data 0×00 to the 14-bit display memory address (0×C0-0×CD) after power-on.
2. The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED. They must not be reversed.

8 Key Scanning

8.1 Key Data Reading



The key scanning is automatically completed by the hardware. Users only need to read the key values in sequence. It takes two display cycles to complete one key scan, with each display cycle approximately taking 4ms. Within 8ms, two different keys were pressed successively, and the key values read twice were those of the first pressed key.

After the host sends the command to read the key, it starts to read the 5-byte key data in sequence. The read key data is output from the lower bit. When a certain key is pressed, the bit position within the corresponding key data byte is 1.

The keys and their corresponding key data are as shown in the following figure:

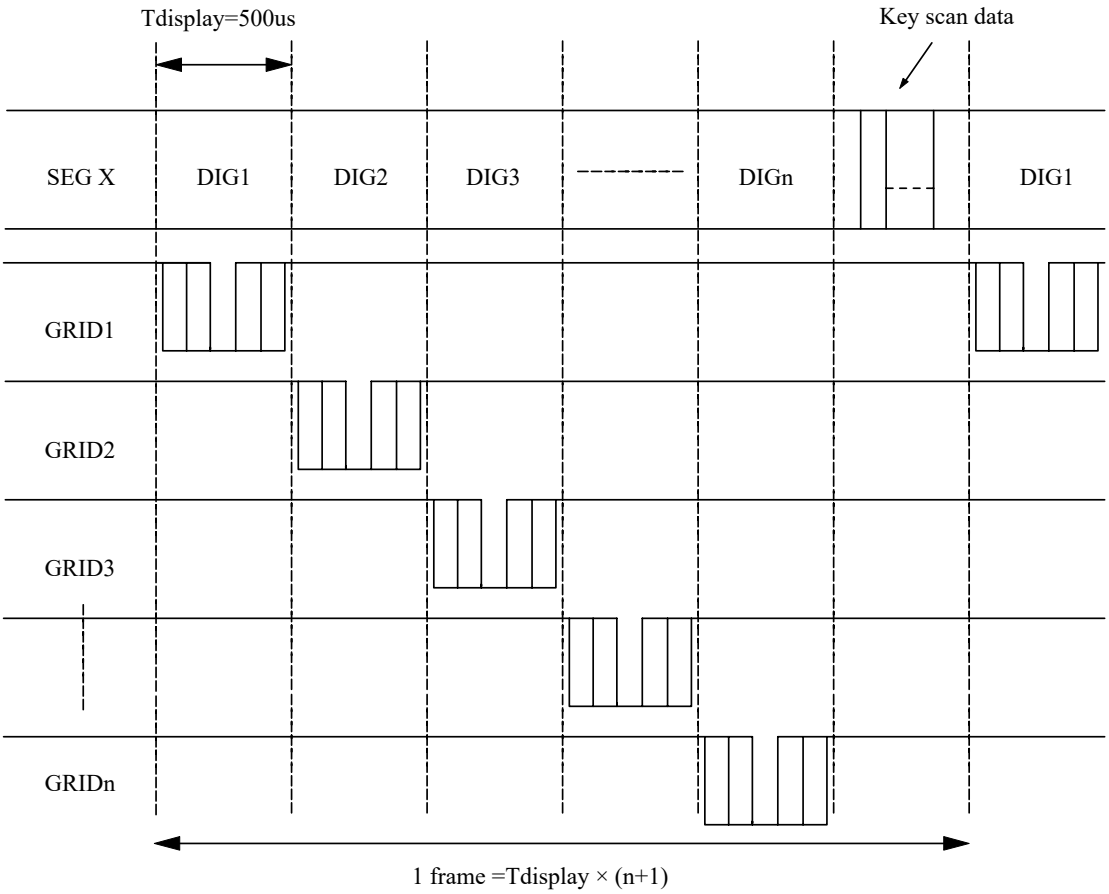
Key data	X	X	X	K2	K1	X	K2	K1
Byte 0	0	0	0	K2/KS2	K1/KS2	0	K2/KS1	K1/KS1
Byte 1	0	0	0	K2/KS4	K1/KS4	0	K2/KS3	K1/KS3
Byte 2	0	0	0	K2/KS6	K1/KS6	0	K2/KS5	K1/KS5
Byte 3	0	0	0	K2/KS8	K1/KS8	0	K2/KS7	K1/KS7
Byte 4	0	0	0	K2/KS10	K1/KS10	0	K2/KS9	K1/KS9
	D7	D6	D5	D4	D3	D2	D1	D0

Note: Reading key data must be done in sequence. Cross-byte reading is not allowed, and the reading should not exceed 5 bytes.

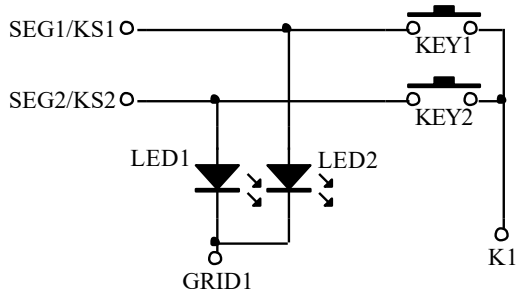
8.2 Key Scan Timing

One cycle of key scanning consists of two frames of display. The first frame shows the cycle scanning of keys KS1-KS8, and the second frame shows the cycle scanning of keys KS9-KS10. The scanning data of the 10×2 matrix keys is stored in RAM.

The key scanning and display sequence diagram is as follows:

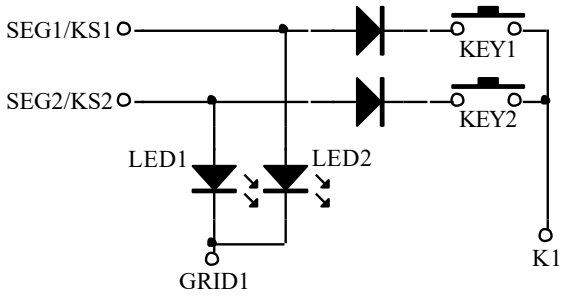


8.3 Key/Display Reuse



As shown in the above figure, for LED1 to be on and LED2 to be off, SEG1 needs to be in the "0" state and SEG2 in the "1" state. If KEY1 and KEY2 are pressed simultaneously, it is equivalent to SEG1 and SEG2 being short-circuited. At this time, both LED1 and LED2 will be on. This can be solved by connecting diodes in series.

As shown in the following figure：



9 Serial Communication Commands

9.1 Communication Interface

3 lines are required to interface with the VK1S68C.

STB is the chip select pin. it is used to enable / disable communication with the controller, high level disable(prohibits and initializes internal timing), low level enables. The first byte input by the DIO pin after the falling edge of the STB is used as the command. If the STB is set to high level during instruction or data transmission, the serial communication is initialized and the command or data being transmitted is invalid.

CLK is the clock signal pin. It reads the data of DIO pin to display RAM on the rising edge and outputs the data to DIO pin on the falling edge.

DIO is the Bidirectional data pin. It used to read / write data or write commands . it is an NMOS open drain output and needs to connect a resistor. with VDD.

9.2 Command Format

The instruction is used to set the display mode, write display data and read key values.

The first byte input by DIO after the falling edge of STB is taken as the instruction. After decoding, the highest two bits, 7 and 6, are selected to distinguish different instructions, as shown in the following table:

bit7	bit6	Function
0	0	Display mode setting command
0	1	Data read and write setting command
1	0	Display control command
1	1	Address setting command

10 Command Description

10.1 Display Mode Setting Command

Set the number of segments and bits for LED display (4 to 7 bits, 10 to 13 segments). When this command is executed, the display is forcibly turned off. If the same mode setting is selected, the command will not be executed. When powered on, the default display mode is 10 segments and 7 bits.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Display mode
0	0	---				0	0	13 seg, 4 bits
0	0					0	1	12 seg, 5 bits
0	0					1	0	11 seg, 6 bits
0	0					1	1	10 seg, 7 bits

10.2 Data Read And Write Setting Commands

This command is used for LED display data writing and key reading as well as related commands. bit1 and bit0 bits are not allowed to be set to 01 or 11. When powered on, the bit3-bit0 data is 0.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Note
0	1	---				0	0	Data read and write mode settings	Write data to display register
0	1					1	0		Read the key data
0	1				0			Address increase mode settings	Automatic address increment
0	1				1				Fixed address
0	1			0				Working mode settings	Normal mode
0	1			1					Test mode

10.3 Address Setting Command

Set the address of the display RAM (0×C0-0×CD). When powered on, the address is set to C0H by default.

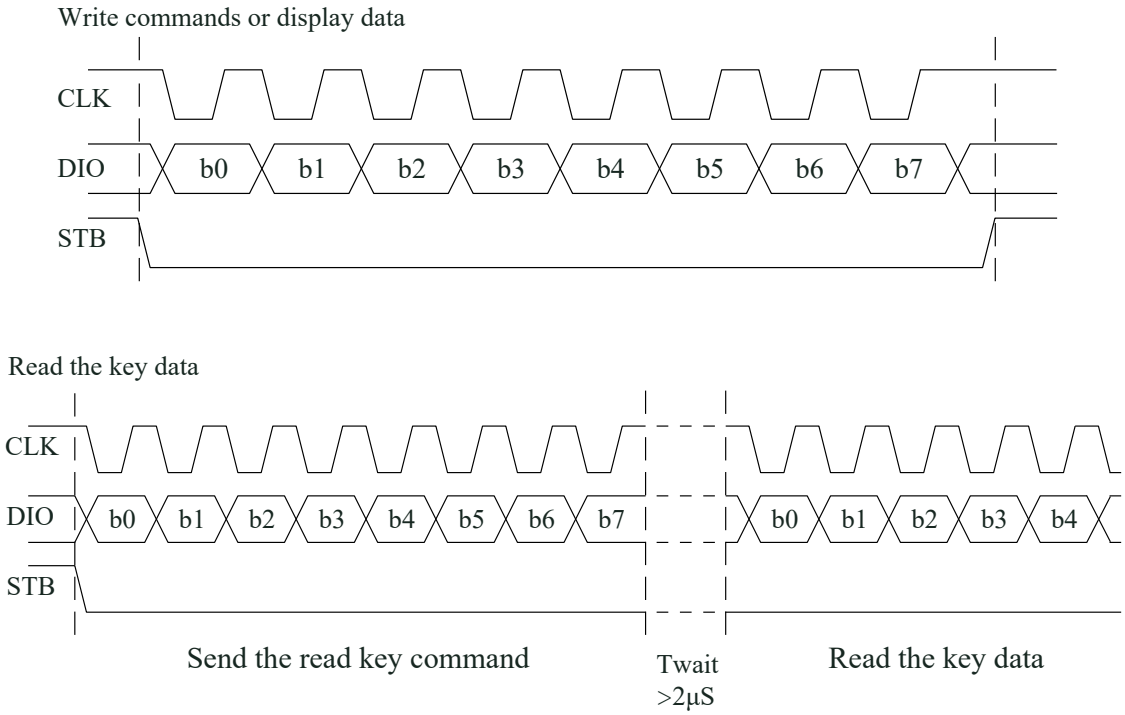
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Display RAM address
1	1	---		0	0	0	0	0xC0
1	1			0	0	0	1	0xC1
1	1			0	0	1	0	0xC2
1	1			0	0	1	1	0xC3
1	1			0	1	0	0	0xC4
1	1			0	1	0	1	0xC5
1	1			0	1	1	0	0xC6
1	1			0	1	1	1	0xC7
1	1			1	0	0	0	0xC8
1	1			1	0	0	1	0xC9
1	1			1	0	1	0	0xCA
1	1			1	0	1	1	0xCB
1	1			1	1	0	0	0xCC
1	1			1	1	0	1	0xCD

10.4 Display Control Command

Set the display switch and select the display brightness (8 levels).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Note
1	0	---			0	0	0	Set the pulse width	Set the pulse width to 1/16
1	0				0	0	1		Set the pulse width to 2/16
1	0				0	1	0		Set the pulse width to 4/16
1	0				0	1	1		Set the pulse width to 10/16
1	0				1	0	0		Set the pulse width to 11/16
1	0				1	0	1		Set the pulse width to 12/16
1	0				1	1	0		Set the pulse width to 13/16
1	0				1	1	1		Set the pulse width to 14/16
1	0			0				Display switch	Show off
1	0			1					Display on

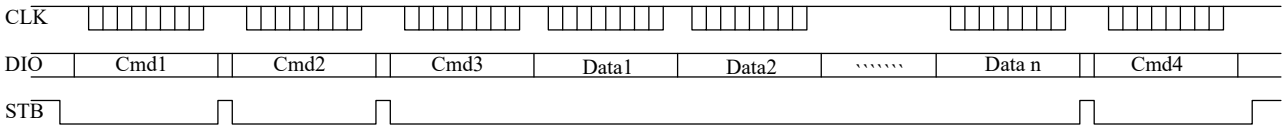
10.5 Command Timing



11 Command Application

11. Send Display Data (address automatically adds 1)

To transfer display data using the address auto-increment mode, first set the starting address of the data to be transferred (corresponding to the display RAM address). After the starting address command word is sent, the STB does not need to be set high and can directly transmit the display data, with a maximum of 14 bytes. Until the last byte of display data is transmitted, the STB is set high.



Cmd1: Display Mode Setting Command - Set the number of segments and bits selected for LED display (can be set during initialization)

Cmd2: Data Read and Write Settings Command - Set Address Auto-increment (0x40)

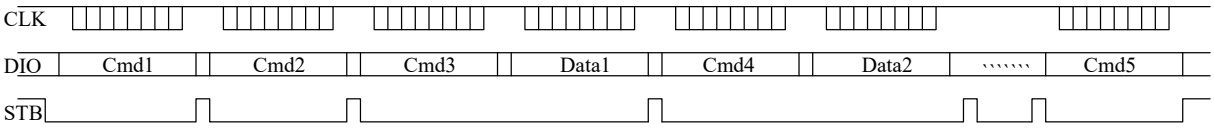
Cmd3: Address Setting Command - Set the display RAM starting address (0xC0-0xCD)

Data1-Datan: Send the display data to the starting address set by Cmd3 and the subsequent display RAM (up to 14 bytes)

Cmd4: Display Control Commands - Display on and set the display brightness level

11.2 Send Display Data (fixed address)

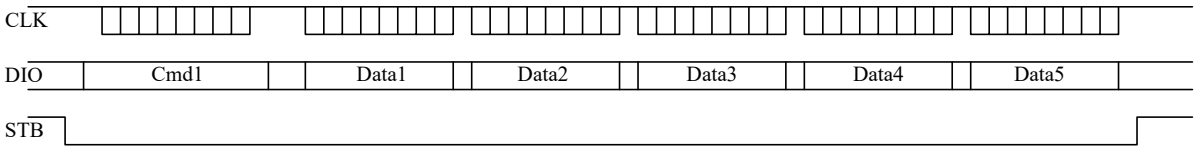
To transfer display data using the fixed address mode, first set the address of the data to be transferred (corresponding to the display RAM address). After the address is sent, the STB does not need to be set high and can directly transfer 1 byte of display data. After the data is transferred, the STB is set high. Send the address of the next display data. The STB does not need to be set high and can directly send 1 byte of display data. After the data is transmitted, the STB is set high. ... Display the data until the last byte is transmitted, with a maximum of 14 bytes.



Cmd1: Display Mode Setting Command - Set the number of segments and bits selected for LED display (can be set during initialization)
Cmd2: Data Read and Write Settings Command - Set Fixed Address Mode (0x44)
Cmd3: Address Setting Command - Set Display RAM Address (0xC0-0xCD)
Data1: Send display data to the display RAM address set by Cmd3
Cmd4: Address Setting Command - Set Display RAM Address (0xC0-0xCD)
Data2: Send display data to the display RAM address.... set in Cmd4 A maximum of 14 bytes of data can be transmitted
Cmd5: Display Control Commands - Display on and set the display brightness level

11.3 Read The Key Data

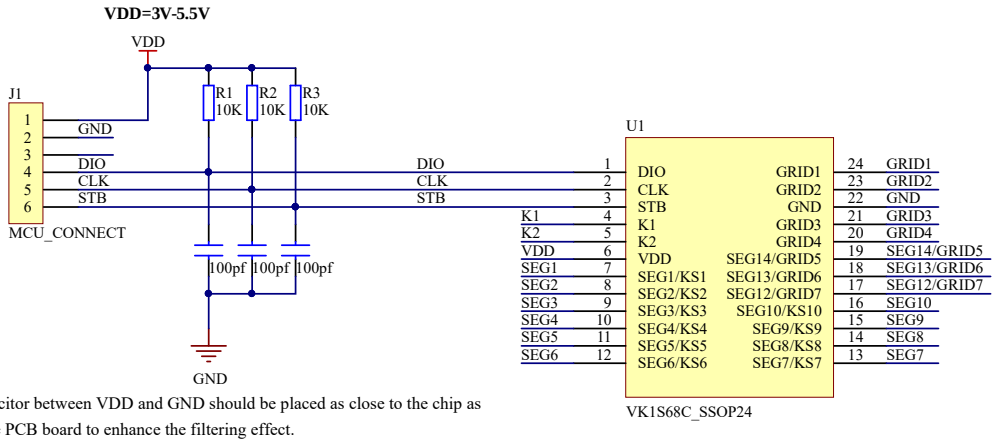
The data read and write setting command is set to read key data, and then start reading 5 bytes of key data in sequence. The read key data is output starting from the lower bit.



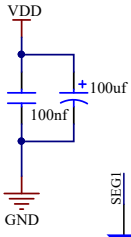
Cmd1: Display Mode Setting Command - Set to read key data (0x42)
Data1-Data5: Sequentially read 5 bytes of key data, and output the key data starting from the lower bit.

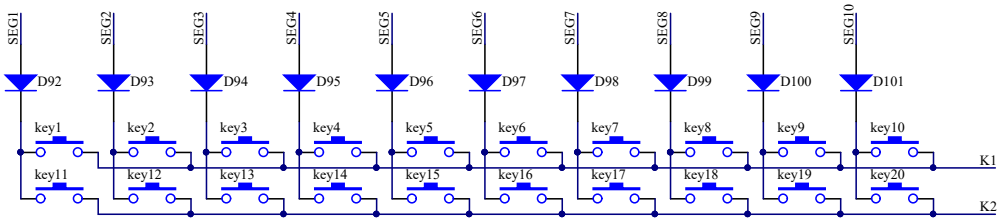
12 Application Circuits

When the surrounding interference is relatively large, a 10R to 10k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin

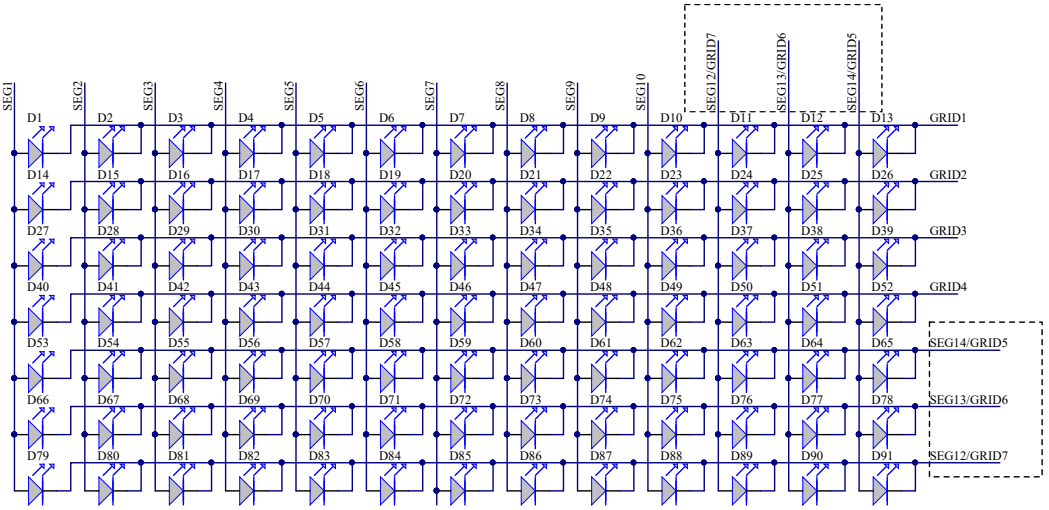


The filter capacitor between VDD and GND should be placed as close to the chip as possible on the PCB board to enhance the filtering effect.





A diode needs to be connected in series for key/display multiplexing



The VK1S68C features multiple display modes and allows for the setting of the number of segments and bits: 10 segments with 7 bits, 11 segments with 6 bits, 12 segments with 5 bits, and 13 segments with 4 bits
Connect the SEG pin to the anode of the LED and the GRID pin to the cathode of the LED

13 Electrical Characteristics

13.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～7.0	V
Input voltage	VIN	V_{SS}-0.5～V_{DD}+0.5	V
Power loss	PD	400	mW
Drive output current	I_{OLGRID}	+250	mA
	I_{OHSEG}	-50	mA
Storage temperature	T_{STG}	-50～+125	℃
Operating temperature	T_{OTG}	-40～+85	℃

13.2 DC Electrical Characteristics

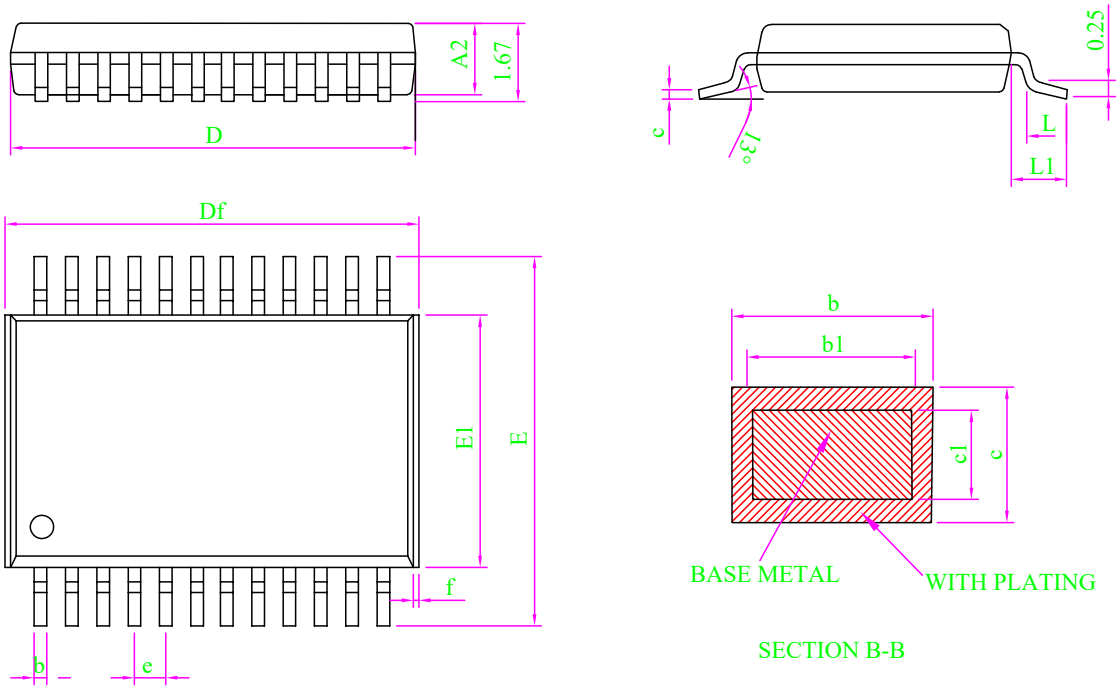
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	3.0	—	5.5	V	—	—
Static current	I_{DD}	—	0.5	1.0	mA	5V	No load /LED off
High-level output current	I_{OHSEG1}	-20	-25	-40	mA	5V	VO=VDD-2V SEG1/KS1- SEG10/KS10 SEG12/GRID7-SEG14/GRID5
	I_{OHSEG2}	-25	-30	-50			VO=VDD-3V SEG1/KS1- SEG10/KS10 SEG12/GRID7-SEG14/GRID5
Low-level input current	I_{OLGRID}	100	140	—	mA	5V	VO=0.3V GRID1- GRID4 SEG14/GRID5-SEG12/GRID7
High-level output current tolerance	I_{TOLSEG}	—	—	5	%	VDD	VO=VDD-3V(VDD=5V) VO=VDD-2V(VDD=3V) SEG1/KS1 to SEG10/KS10, SEG12/GRID7 to SEG14/GRID5
Low-level Input	V_{IL}	0	—	0.3	VDD	VDD	STB, CLK, DIO
High-level Input	V_{IH}	0.7	—	1.0		VDD	
Pull-down resistor	R_L	40	—	100	kΩ	5V	—

13.3 AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Transmission delay time	t_{PLZ}	—	—	300	nS	CLK → DOUT CL = 15pF, RL = 10KΩ
	t_{PZL}	—	—	100	nS	
Rising time	t_{ZH1}	—	—	2	μS	CL=300pF SEG1-SEG10
	t_{ZH2}	—	—	0.5	μS	CL=300pF GRID1-GRID4 SEG12/GRID7～SEG14/GRID5
fall time	t_{THZ}	—	—	1.5	μS	CL=300pF SEGn,GRIDn
Maximum input clock frequency	F_{MAX}	—	—	1	MHz	Duty cycle: 50%
Input capacitance	C_I	—	—	15	pF	—

14 Package Information

14.1 SSOP24 (150mil) (8.65mm × 3.90mm PP=0.635mm)



Note:

1. All dimension are in mm.
2. Dim D&El does not include plastic flash; Df includes plastic flash(f);
Flash: Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.007mm-0.015mm

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.20
A2	1.35	1.45	1.55
b	0.23	-	0.31
b1	0.22	0.25	0.28
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	8.56	8.66	8.76
Df	8.66	-	9.16
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635 BSC		
L	0.51	0.66	0.81
L1	0.95	1.05	1.15
θ	0	-	8°
f	0.05	-	0.20

15 Disclaimer

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Applicability —— This product is not designed or intended for use in life-critical, medical, or safety systems where failure could result in injury or death. The customer shall assume full responsibility for any such use.

Application —— All product application descriptions provided herein are intended for illustrative purposes only.
The Company makes no representations or warranties, express or implied, regarding the suitability of any specific application without further testing or modification.

The customer is solely responsible for determining whether the Company's products are appropriate for their intended applications or end customers.

The customer shall ensure proper design practices, implementation safeguards, and operational validation to minimize risks associated with product use.

The Company shall not be held liable for any defects, losses, costs, or damages arising from weaknesses or failures in the customer's own products or applications, or from the integration or use of third-party products.

Furthermore, the customer shall conduct all necessary testing and validation for any third-party deployment of the Company's products to avoid potential misuse or associated damages. The Company assumes no liability in this regard.

Commercial terms of sale —— Unless otherwise agreed in writing, sales of this product are subject to the Company's standard terms and conditions of sale. The Company expressly rejects the applicability of the customer's general terms and conditions.

Export control—— This product may be subject to applicable export control regulations. The customer is solely responsible for compliance with such regulations, including obtaining any necessary export licenses.

16 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-09-18	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/