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VK1616 Datasheet

7×4 LED DRIVER

Rev.1.3

1 General Description

VK1616 is a dedicated chip for digital tube or dot matrix LED driver control, which integrates a 3-wire serial interface, data latch, LED driver and other circuits internally. The SEG pin is connected to the anode of the LED, and the GRID pin is connected to the cathode of the LED, which can support a dot matrix LED display panel of 7SEG×4GRID. Adopt the SOP16 packaging form.

2 Key Features

- Operating voltage：3.0-5.5V
- Built-in RC oscillator
- 7 SEG pins and 4 GRID pins
- The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED
- 3-wire serial interface
- The overall brightness is adjustable at 8 levels
- The display mode is 7SEG×4GRID
- Built-in power-on reset circuit Strong anti-interference ability
- Available Packages:
  SOP16(150mil)(9.90mm × 3.90mm PP=1.27mm)

3 Application Field

- Small household appliances
- Induction cooker/microwave oven
- Pressure gauge

4 Product Selection

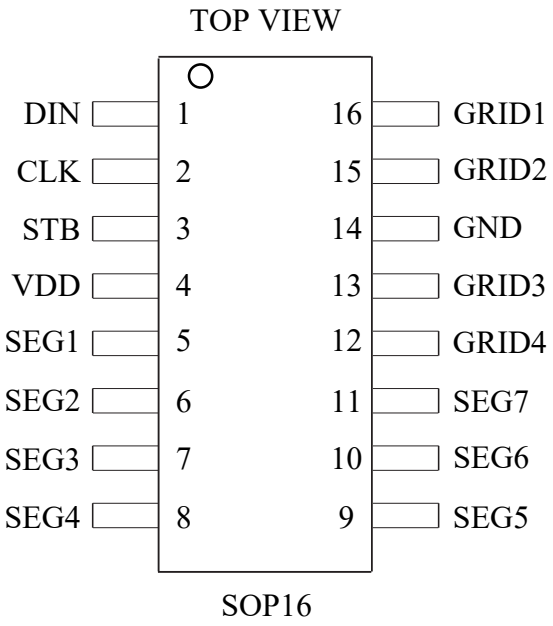
Part No.	Common Cathode Drive	Common Anode Drive	Key press	Packaging
VK1616	7 / 4	4 / 7	---	SOP16
VK1618	5 / 7 , 6 / 6 7 / 5 , 8 / 4	7 / 5 , 6 / 6 5 / 7 , 4 / 8	5×1	SOP18
VK1620	8 / 6 , 9 / 5 10 / 4	6 / 8 , 5 / 9 4 / 10	---	SOP20
VK1624	11 / 7 , 12 / 6 13 / 5 , 14 / 4	7 / 11 , 6 / 12 5 / 13 , 4 / 14	---	SOP24
VK1S68C	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	SSOP24
VK1Q68D	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	QFN24L (4mm*4mm）
VK1668	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	SOP24
VK1668B	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	SSOP24
VK1628	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	SOP28
VK1628A	10 / 7 , 11 / 6 12 / 5 , 13 / 4	7 / 10 , 6 / 11 5 / 12 , 4 / 13	10×2	SSOP28

Note: For both common cathode and common anode digital tubes, SEG is connected to the anode and GRID to the cathode.

5 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel) Qty	Box Qty	Total Qty	Notes
VK1616	SOP16	50/tube		10000/box	100000 PCS	
VK1618	SOP18					
VK1620	SOP20	36/tube		2880/box	28800 PCS	
VK1624	SOP24	30/tube		2400/box	24000 PCS	
VK1S68C	SSOP24	50/tube		10000/box	100000 PCS	
VK1Q68D	QFN24L (4mm*4mm)		3000/reel		24000 PCS	reel
VK1668	SOP24	30/tube		2400/box	24000 PCS	
VK1668B	SSOP24	50/tube		10000/box	100000 PCS	
VK1628	SOP28	26/tube		2080/box	20800 PCS	
VK1628A	SSOP28	50/tube		5000/box	50000 PCS	

6 Package Pinout Information(SOP16)



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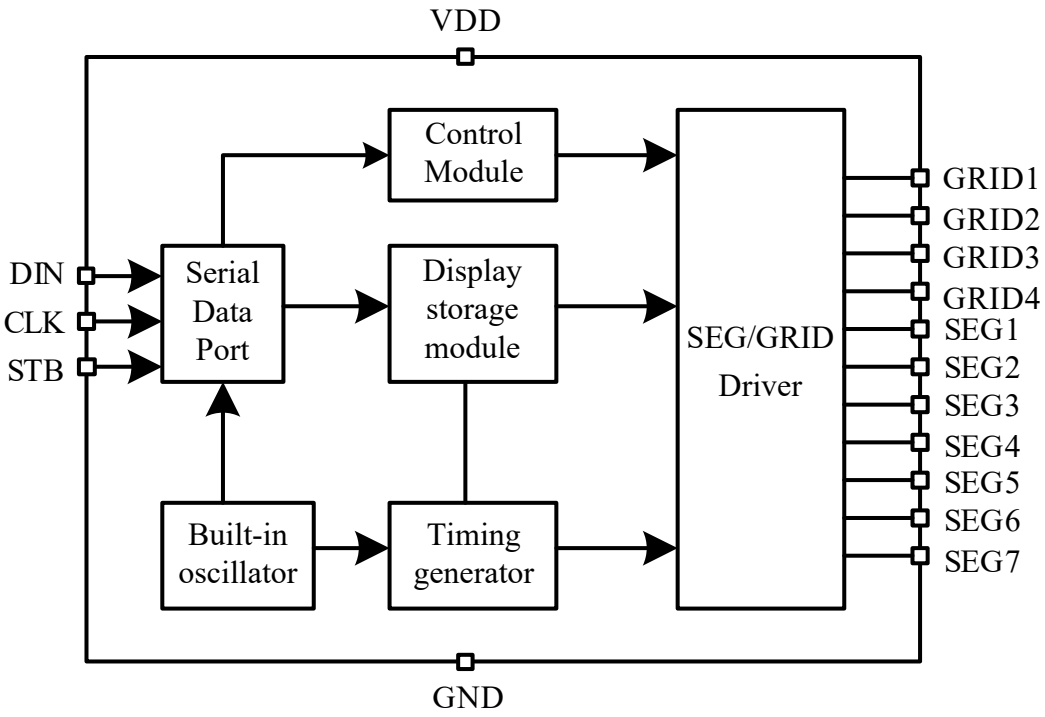
6.1 VK1616/SOP16 Pin Description

No.	Name	I/O	Function
1	DIN	I	Serial data is input at the rising edge of the clock
2	CLK	I	The clock signal reads serial data to the display RAM at the rising edge and outputs data at the falling edge
3	STB	I	Chip selection signal, high level disabled, low level enabled
4	VDD	VDD	Positive power supply
5～11	SEG1-SEG7	O	LED SEG output (P-channel)
12,13, 15,16	GRID4- GRID1	O	LED GRID output (N-channel open-drain output)
14	GND	GND	Negative power supply

7 Functional Description

7.1 Block Diagram



7.2 Display RAM- Storage Structure

The static display memory (RAM) structure is 7x4 bits and stores the displayed data. The content of RAM is directly mapped to the display content of the LED driver, with the display addresses being 0xC0,0xC2,0xC4, and 0xC6. If you want to turn on or off a certain LED, simply set the corresponding display RAM position 1 or clear 0. For example, to control the on/off of LED1 driven by pins SEG1 and GRID1, simply set the Bit0 position of the corresponding display RAM (address 0xC0) to 1 or clear 0. Clear the RAM bits corresponding to the unused SEG pins in the application to 0.

The process of mapping the contents in RAM to LED is shown in the following table:

SEG / GRID	X	X	X	X	X	X	X	X	Addr	X	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	Addr	SEG / GRID
GRID1									0xC1								LED1	0xC0	GRID1
GRID2									0xC3									0xC2	GRID2
GRID3									0xC5									0xC4	GRID3
GRID4									0xC7									0xC6	GRID4
	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0		

Note:

The value stored inside the chip display RAM at the moment of power-on may be random. It is recommended that the customer perform a power-on reset of the display RAM, that is, write all the data 0x00 to the display memory address (0xC0,0xC2,0xC4,0xC6) after power-on.

The SEG pin can only be connected to the anode of the LED, and the GRID pin can only be connected to the cathode of the LED. They must not be reversed.

8 Serial Communication Commands

8.1 Communication Interface

3 lines are required to interface with the VK1616.

STB is the chip select pin. it is used to enable / disable communication with the controller, high level disable(prohibits and initializes internal timing), low level enables. The first byte input by the DIO pin after the falling edge of the STB is used as the command. If the STB is set to high level during instruction or data transmission, the serial communication is initialized and the command or data being transmitted is invalid.

CLK is the clock signal pin. It reads the data of DIO pin to display RAM on the rising edge and outputs the data to DIO pin on the falling edge.

DIN is the data input pin. Input serial data on the rising edge of the clock, starting from the low bit.

8.2 Command Format

The instructions are used to set the display mode and the status of the LED driver.

The first byte input by DIN after the falling edge of STB is regarded as an instruction. After decoding, the highest two bits B7 and B6 are taken to distinguish different instructions.

B7	B6	Instruction
0	0	Display mode Settings
0	1	Data command Settings
1	0	Display control command Settings
1	1	Address command Settings

9 Command Description

9.1 Display Mode Setting Command

This command is used to set the number of selected segments and bits. Although VK1616 does not have a segment multiplexing pin, when writing programs, the mode command needs to be written as 7 seg and 4 bits. When the instruction is executed, the display is forcibly closed. To send a display control command to start the display, the originally displayed data content will not be changed. However, when the same mode is set, the above situation will not occur. The default power-on setting mode is 7-seg 7-bit. It needs to be set to 7-seg 4-bit.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Display mode
0	0	————				0	0	7-seg 4-bit

9.2 Data Write Setting Command

This instruction is used to set data writing and reading. Bits B1 and B0 are not allowed to be set to 01 or 11.

When powered on, the Bit3-Bit0 data is 0.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Note
0	1	---				0	0	Data write mode settings	Write the data to the display register
0	1				0			Address increase mode settings	The address increases automatically
0	1				1				Fixed address
0	1			0				Working mode Settings	Normal mode
0	1			1					Test mode

9.3 Address Setting Command

Set the address of the displayed RAM (0xC0,0xC2,0xC4,0xC6). When powered on, the address is set to C0H by default.

B7	B6	B5	B4	B3	B2	B1	B0	Video memory address
1	1	————		0	0	0	0	00H
1	1			0	0	1	0	02H
1	1			0	1	0	0	04H
1	1			0	1	1	0	06H

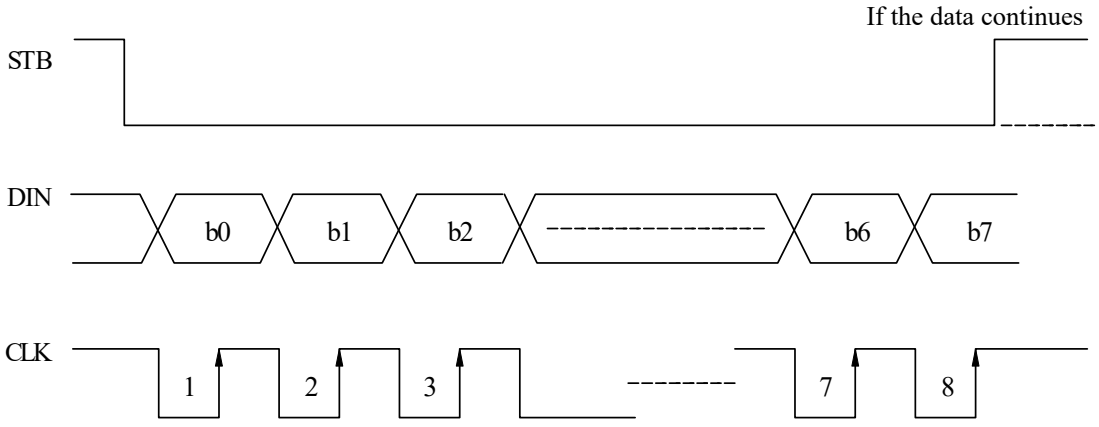
9.4 Display Control Command

Set the display switch and select the display brightness (8 levels).

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Function	Note
1	0				0	0	0	Set the pulse width	Set the pulse width to 1/16
1	0				0	0	1		Set the pulse width to 2/16
1	0				0	1	0		Set the pulse width to 4/16
1	0				0	1	1		Set the pulse width to 10/16
1	0				1	0	0		Set the pulse width to 11/16
1	0				1	0	1		Set the pulse width to 12/16
1	0				1	1	0		Set the pulse width to 13/16
1	0				1	1	1		Set the pulse width to 14/16
1	0			0				Display switch	Show off
1	0			1					Display on

9.5 Command Timing

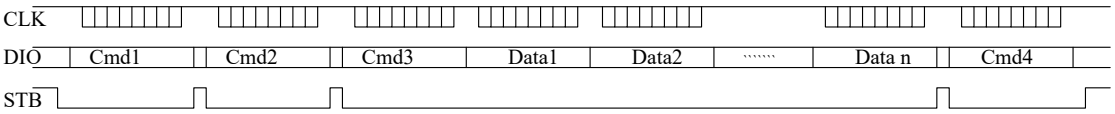
When STB is at a low level, the chip operates at the rising edge of the clock when receiving one BIT. Data receiving (writing data) sequence diagram



10 Command Application

10.1 Display Data (address is automatically incremented by 1)

To transfer display data using the address auto-increment mode, first set the starting address of the data to be transferred (corresponding to the display RAM address). After the starting address command word is sent, the STB does not need to be set high and can directly transmit the display data, with a maximum of 0xC0,0xC2,0xC4, and 0xC6. Until the last byte of display data is transmitted, the STB is set high.



Cmd1: Display Mode Setting Command - Set the number of segments and bits selected for LED display (can be set during initialization)

Cmd2: Data Read and Write Settings Command - Set Address Auto-increment (0x40)

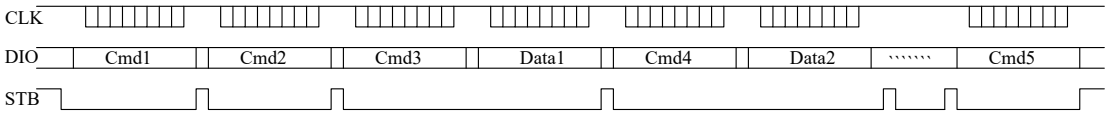
Cmd3: Address Setting Command - Set the starting address of the display RAM (0xC0,0xC2,0xC4,0xC6). Data1-Datan: Send display data to the starting address set by Cmd3 and the subsequent display RAM. Cmd4: Display control command - Open the display and set the display brightness level

Note: When writing data, the RAM address is automatically increments by 1, and zeros are sent between discontinuous addresses for padding.

For example: Send data data0-data3
data0->0xC0 0->0xC1 data1->0xC2 0->0xC3 data2->0xC4 0->0xC5 data3->0xC6

10.2 Send Display Data (fixed address)

To transfer display data using the fixed address mode, first set the address of the data to be transferred (corresponding to the display RAM address). After the address is sent, the STB does not need to be set high and can directly transfer 1 byte of display data. After the data is transferred, the STB is set high. Send the address of the next display data. The STB does not need to be set high and can directly send 1 byte of display data. After the data is transmitted, the STB is set high. ... Display the data until the last byte is transmitted.



Cmd1: Display Mode Setting Command - Set the number of segments and bits selected for LED display (can be set during initialization)

Cmd2: Data Read and Write Settings Command - Set Fixed Address Mode (0x44)

Cmd3: Address Setting Command - Set the display RAM address (0xC0,0xC2,0xC4,0xC6)

Data1: Send display data to the display RAM address set by Cmd3

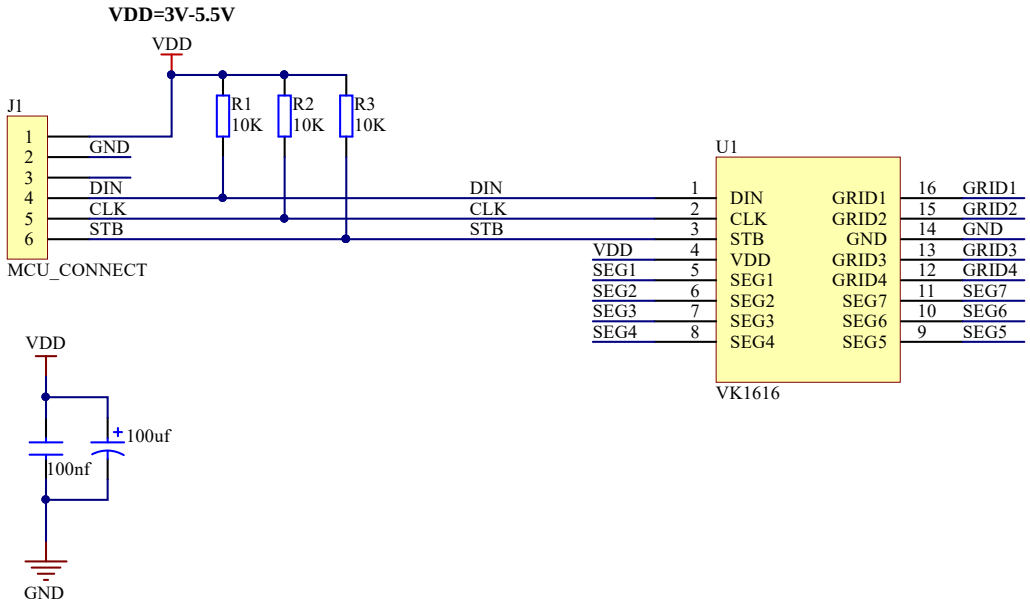
Cmd4: Address Setting Command - Set the display RAM address (0xC0,0xC2,0xC4,0xC6)

Data2: Send display data to the display RAM address.... set in Cmd4 A maximum of 4 bytes of valid data can be transmitted

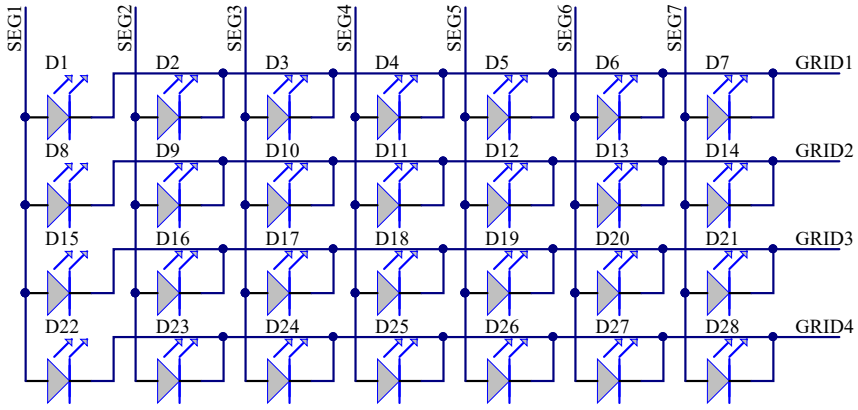
Cmd5: Display Control Commands - Display on and set the display brightness level

11 Application Circuits

When the surrounding interference is relatively large, a 10R to 10k resistor and a PF-level small capacitor to ground can be connected in series on the communication pin. When the power supply of the single-chip microcomputer (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit on the communication pin



The filter capacitor between VDD and GND should be placed as close to the chip as possible on the PCB board to enhance the filtering effect.



Connect the SEG pin to the anode of the LED and the GRID pin to the cathode of the LED

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～7.0	V
Input voltage	VIN	V_{SS}-0.5～V_{DD}+0.5	V
Power loss	PD	400	mW
Drive output current	I_{OLGRID}	+250	mA
	I_{OHSEG}	-50	mA
Storage temperature	T_{STG}	-50～+125	℃
Operating temperature	T_{OTG}	-40～+85	℃

12.2 DC Electrical Characteristics

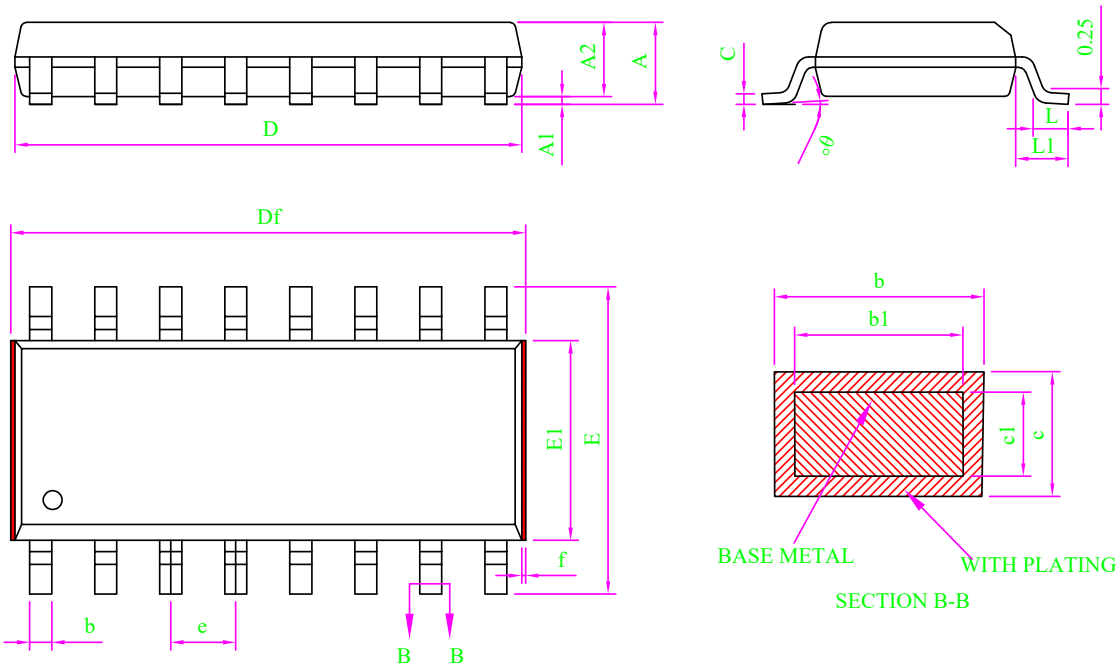
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	3.0	—	5.5	V	—	—
Static current	I_{DD}	—	0.5	1.0	mA	5V	No load /LED off
High-level output current	I_{OHSEG1}	-20	-25	-40	mA	5V	VO=VDD-2V SEG1- SEG7
	I_{OHSEG2}	-25	-30	-50			VO=VDD-3V SEG1- SEG7
Low-level input current	I_{OLGRID}	100	140	—	mA	5V	VO=0.3V GRID1- GRID4
High-level output current tolerance	I_{TOLSEG}	—	—	5	%	VDD	VO=VDD-3V(VDD=5V) VO=VDD-2V(VDD=3V) SEG1 to SEG7
Low-level Input	V_{IL}	0	—	0.3	VDD	VDD	STB, CLK, DIO
High-level Input	V_{IH}	0.7	—	1.0		VDD	
Pull-down resistor	R_L	—	—	—	kΩ	5V	—

12.3 AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Transmission delay time	t_{PLZ}	—	—	300	nS	CLK → DOUT CL = 15pF, RL = 10KΩ
	t_{PZL}	—	—	100	nS	
Rising time	t_{ZH1}	—	—	2	μS	CL=300pF SEG1-SEG7
	t_{ZH2}	—	—	0.5	μS	CL=300pF GRID1-GRID4
fall time	t_{THZ}	—	—	1.5	μS	CL=300pF SEGn,GRIDn
Maximum input clock frequency	F_{MAX}	—	—	1	MHz	Duty cycle: 50%
Input capacitance	C_I	—	—	15	pF	—

13 Package Information

13.1 SOP16(9.9mm × 3.9mm PP=1.27mm)



Note:

1. All dimension are in mm.
   Dim D&El does not include plastic flash; Df includes plastic flash(f);
   Flash: Plastic residual around body edge after de junk/singulation.
2. Dim b does not include dambar protrusion/intrusion.
3. Plating thickness 0.007mm-0.020mm

MILLIMETER			
SYMBOL	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	0.15	0.20
A2	1.35	1.45	1.55
b	0.39	-	0.47
b1	0.38	0.41	0.43
c	0.20	-	0.25
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
Df	9.90	-	10.40
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.51	0.66	0.81
L1	0.95	1.05	1.15
θ	0	-	8°
f	0.05	-	0.20

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15 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-09-04	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

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