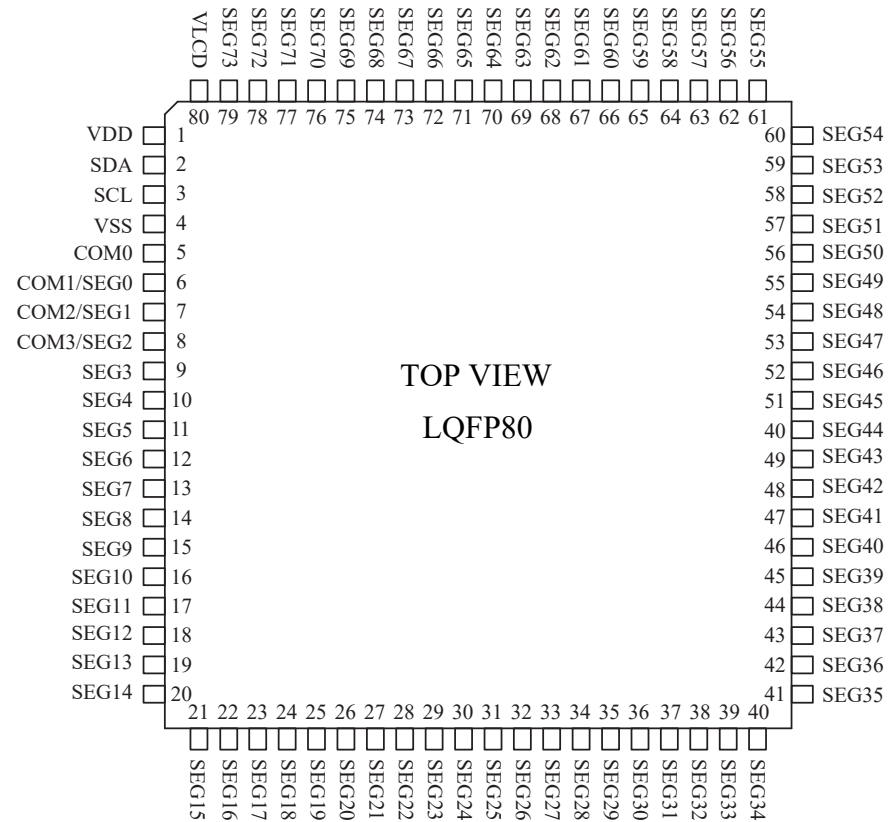


14	SEG8	70*70	93.36	867.92	
15	SEG9	70*70	93.36	783.42	
16	SEG10	70*70	93.36	698.92	
17	SEG11	70*70	93.36	614.42	
18	SEG12	70*70	93.36	529.92	
19	SEG13	70*70	93.36	445.42	
20	SEG14	70*70	93.36	360.92	
21	SEG15	70*70	93.36	276.42	
22	SEG16	70*70	93.36	191.92	
23	SEG17	70*70	93.36	107.42	
24	SEG18	70*70	368.04	93.36	
25	SEG19	70*70	452.54	93.36	
26	SEG20	70*70	537.04	93.36	
27	SEG21	70*70	621.54	93.36	
28	SEG22	70*70	706.04	93.36	
29	SEG23	70*70	790.54	93.36	
30	SEG24	70*70	875.04	93.36	
31	SEG25	70*70	959.54	93.36	
32	SEG26	70*70	1044.04	93.36	
33	SEG27	70*70	1128.54	93.36	
34	SEG28	70*70	1213.04	93.36	
35	SEG29	70*70	1297.54	93.36	
36	SEG30	70*70	1382.04	93.36	
37	SEG31	70*70	1466.54	93.36	
38	SEG32	70*70	1551.04	93.36	
39	SEG33	70*70	1635.54	93.36	
40	SEG34	70*70	1906.64	107.42	
41	SEG35	70*70	1906.64	191.92	
42	SEG36	70*70	1906.64	276.42	
43	SEG37	70*70	1906.64	360.92	
44	SEG38	70*70	1906.64	445.42	
45	SEG39	70*70	1906.64	529.92	
46	SEG40	70*70	1906.64	614.42	
47	SEG41	70*70	1906.64	698.92	
48	SEG42	70*70	1906.64	783.42	

6 Package Pinout Information(LQFP80)



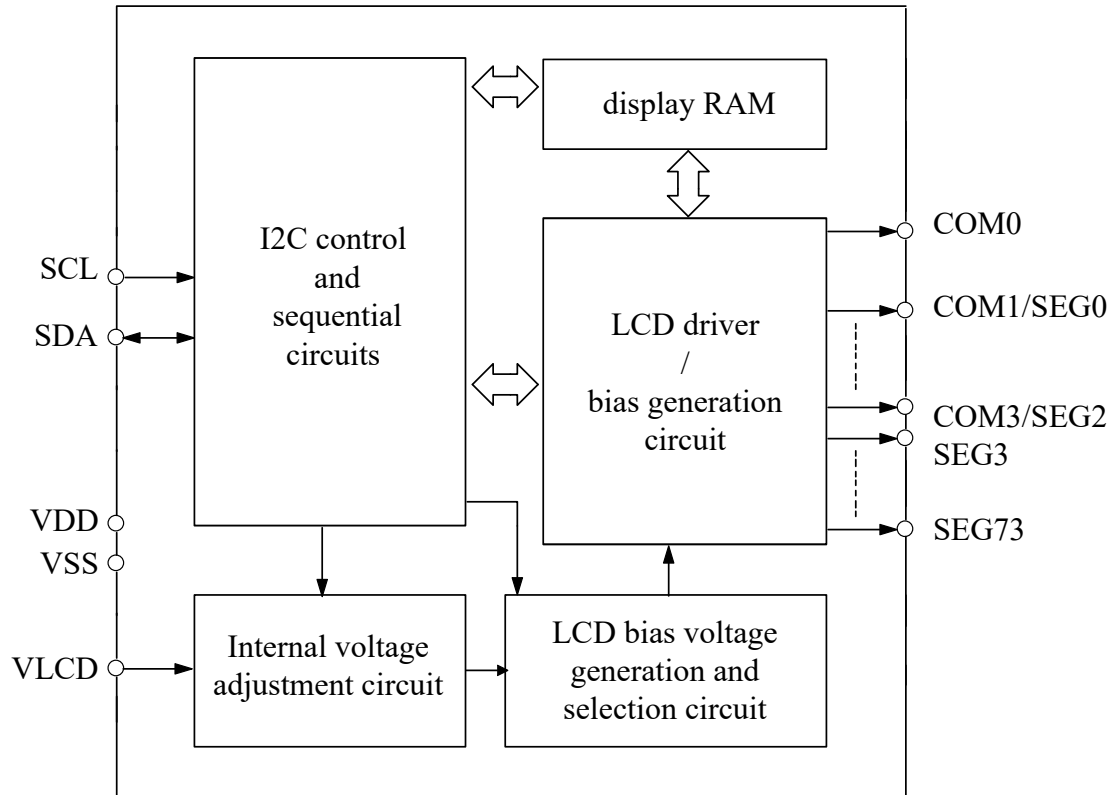
For more information: [Page 24](#)

6.1 VKS146/LQFP80 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	Positive power supply
2	SDA	I/O	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	Negative power supply
5	COM0	O	LCD COM drive outputs
6-8	COM1/SEG0- COM3/SEG2	O	LCD COM/SEG drive outputs, software configuration: 1COM or 2/3/4COM
9-79	SEG3-SEG73	O	LCD SEG drive outputs
80	VLCD	I	When the VLCD pin and VDD pin are short-circuited and the internal voltage regulation function is enabled, the drive voltage is regulated by the internal voltage regulation function. When the VLCD pin is connected in series with the VDD pin and the internal voltage adjustment function is disabled, the LCD driving voltage is set by the series resistor.

7 Functional Description

7.1 Block Diagram



7.2 Display RAM

The static display memory (RAM) structure is 71×4 bits (74×1 bits for 1COM, $73 \times$ bits for 2COM, and 72×3 bits for 3COM), storing the displayed data. The content of the RAM is directly mapped to the display content of the LCD driver. Access the data in the display RAM via I2C commands.

The following is a mapping from the RAM to the LCD pattern:

1COM Output				COM0	1COM Output				COM0	Addr
2COM Output			COM1	COM0	2COM Output			COM1	COM0	Addr
3COM Output		COM2	COM1	COM0	3COM Output		COM2	COM1	COM0	Addr
4COM Output	COM3	COM2	COM1	COM0	4COM Output	COM3	COM2	COM1	COM0	Addr
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
SEG7					SEG6					03H
SEG9					SEG8					04H
SEG11					SEG10					05H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
					SEG74					25H
	D7	D6	D5	D4		D3	D2	D1	D0	Data

RAM Mapping of 71×4

7.3 System Oscillator

The clock of VK2C24A is used to generate LCD drive signals and internal logic timing. The system clock is derived from the internal RC oscillator (32kHz), and the system clock frequency (f_{SYS}) determines the LCD frame frequency.

The system setting command can start or stop the system oscillator. After the display shows off and the system oscillator stops, the system enters the power-saving mode.

When the system is powered on and working, the system oscillator is in a stopped state.

The Settings of the system oscillation are shown in the following figure:



7.4 LCD operating voltage

The LCD driver voltage can be obtained through the VLCD pin or selected as a 16-level voltage through the internal configuration.

When the VLCD pad is connected to the VCCA2 pad, the LCD driving voltage can be supplied from an external voltage source ($VLCD \leq 5.5V$), and VLCD may be higher than VDD.

When the VDD pad is connected to the VCCA2 pad, the LCD driving voltage can be obtained by connecting the VLCD pin to VDD through a series resistor ($VLCD \leq VDD$).

The internal 16-level voltage is set through a 4-bit programmable analog switch, as shown in the following table: When VCCA2 pad is connected to VDD pad

Bias DA3~DA0	1/1	1/2	1/3	1/4	1/5	Note
00H	1.000	1.000	1.000	1.000	1.000	Default
01H	0.849	0.918	0.944	0.957	0.966	
02H	0.738	0.849	0.894	0.918	0.934	
03H	0.652	0.789	0.849	0.882	0.904	
04H	0.584	0.738	0.808	0.849	0.875	
05H	0.529	0.692	0.771	0.818	0.849	
06H	0.484	0.652	0.738	0.789	0.824	
07H	0.446	0.616	0.707	0.763	0.801	
08H	0.413	0.584	0.678	0.738	0.779	
09H	0.385	0.556	0.652	0.714	0.758	
0AH	0.360	0.529	0.628	0.692	0.738	
0BH	0.338	0.506	0.605	0.672	0.719	
0CH	0.319	0.484	0.584	0.652	0.701	
0DH	0.302	0.464	0.565	0.634	0.684	
0EH	0.287	0.446	0.547	0.616	0.668	
0FH	0.273	0.429	0.529	0.600	0.652	

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3~6.5	V
Input Voltage	VIN	VSS-0.3~VDD+0.3	V
Storage Temperature	TSTG	-50~+125	°C
Operating Temperature	TOTG	-40~+85	°C

12.2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.5	V	—	—
Operating current	IDD1	—	25	40	μA	3V	No load, VLCD=VDD, 1/3 bias, fLCD=80Hz, LCD off, Internal osc on, DA0~DA3 = "0000"
		—	35	50		5V	
Operating current	IDD2	—	2	5	μA	3V	No load, VLCD=VDD, 1/3 bias, fLCD=80Hz, LCD off, Internal osc on, DA0~DA3 = "0000"
		—	4	10		5V	
Standby Current	ISTB	—	—	1	μA	3V	No load, VLCD=VDD LCD off Internal osc off
		—	—	2		5V	
Low-level Input	VIL	0	—	0.3	VDD	3V 5V	SCL, SDA
High-level Input	VIH	0.7	—	1.0	VDD	3V 5V	SCL, SDA
Low Level Output Current	IOL	3.0	—	—	mA	3V	VOL=0.4V SDA
		6.0	—	—		5V	
LCD COM Sink Current	IOL1	250	400	—	μA	3V	VOL=0.3V
		500	800	—		5V	VOL=0.5V
LCD COM Source Current	IOH1	-140	-230	—	μA	3V	VOH=2.7V
		-300	-500	—		5V	VOH=4.5V
LCD SEG Sink Current	IOL2	250	400	—	μA	3V	VOL=0.3V
		500	800	—		5V	VOL=0.5V
LCD SEG Source Current	IOH2	-140	-230	—	μA	3V	VOH=2.7V
		-300	-500	—		5V	VOH=4.5V

13 AC Electrical Characteristics

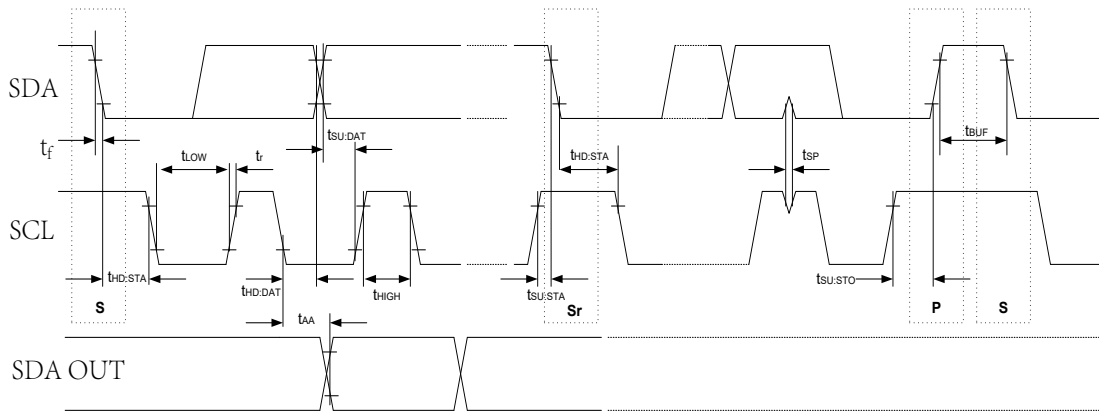
Frame Frequency

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD Frame Frequency	f _{LCD1}	72	80	88	Hz	4.0V	1/4 duty, 25°C
LCD Frame Frequency	f _{LCD2}	144	160	176	Hz	4.0V	1/4 duty, 25°C
LCD Frame Frequency	f _{LCD3}	52	80	124	Hz	4.0V	1/4 duty, -40 ~ +85°C
LCD Frame Frequency	f _{LCD4}	104	160	248	Hz	4.0V	1/4 duty, -40 ~ +85°C

I2C parameter

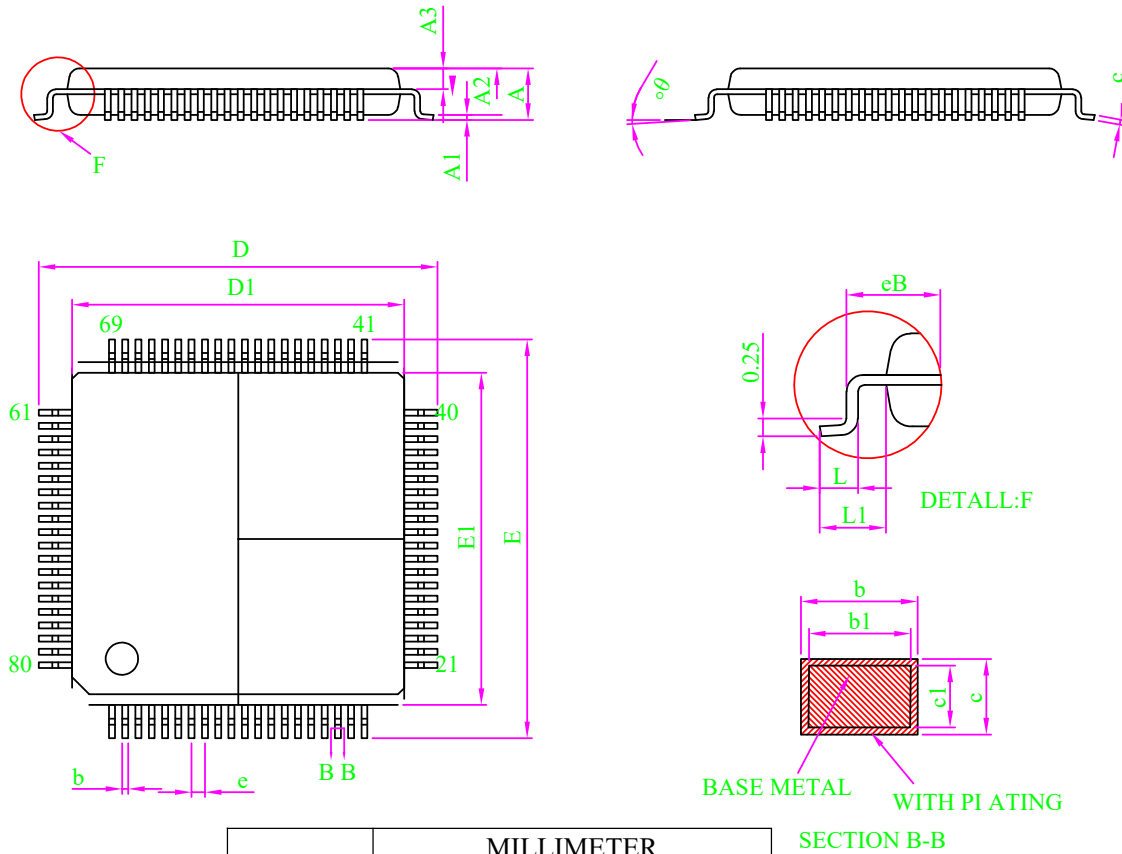
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	f _{SCL}	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	t _{BUF}	1.3	—	—	μs	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	t _{HD:STA}	0.6	—	—	μs	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	t _{LOW}	1.3	—	—	μs	3.0-5.5V	—
SCL High Time	t _{HIGH}	0.6	—	—	μs	3.0-5.5V	—
Start Condition Setup Time	t _{SU:STA}	0.6	—	—	μs	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	t _{HD:DAT}	0	—	—	ns	3.0-5.5V	—
Data Setup Time	t _{SU:DAT}	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	t _R	—	—	0.3	μs	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	t _F	—	—	0.3	μs	3.0-5.5V	periodically sampled
Stop Condition Setup Time	t _{SU:STO}	0.6	—	—	μs	3.0-5.5V	—
Output Valid from Clock	t _{AA}	—	—	0.9	μs	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin)	t _{SP}	—	—	50	ns	3.0-5.5V	Noise suppression time

I²C Timing



14 Package Information

14.1 LQFP80(10.0mm × 10.0mm PP=0.4mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.14	-	0.22
b1	0.13	0.16	0.19
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
eB	11.05	-	11.25
e	0.40 BSC		
L	0.45	-	0.75
L1	1.00 REF		
θ	0	-	7°

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16 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2022-08-10	Initial release	YES
2	1.1	2025-08-30	Change Description	YES

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