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Vinka Microelectronics

# VKL280 Datasheet

35×8 LCD DRIVER

Rev.1.1

# 1 General Description

VKL280 is a universal LCD driver chip that can support LCD screens with a maximum of 280 points (35SEG × 8COM). The single-chip microcontroller can configure display parameters and read/write display data through the I2C interface. Its high anti-interference and ultra-low power consumption features make it suitable for water, electricity, gas meters and industrial control instrument products.

# 2 Key Features

- Operating voltage：2.5-5.5V
- Built-in 25.6 kHz RC oscillator
- Selectable LCD bias:1/4
- Selectable LCD duty:1/8
- Built-in 35×8-bit display RAM
- I2C communication interface
- Built-in EVR (Electrical Volume Register) function
- VLCD voltage range 2.5V~5.5V
- The frame frequency can be configured as 80Hz or 71Hz、64Hz、53Hz
- 4 power modes can be configured
- No need for external components
- Low power consumption, high EMC performance
- Available Packages:
  TSSOP48(240mil)(12.5mm × 6.1mm PP=0.5mm)
  LQFP48(7.0mm × 7.0mm PP=0.5mm)

# 3 Application field

- Electric meter, water meter, gas meter, telephone, fax machine
- Toys
- Handheld instrument
- Alarm clock

## 4 Product Selection

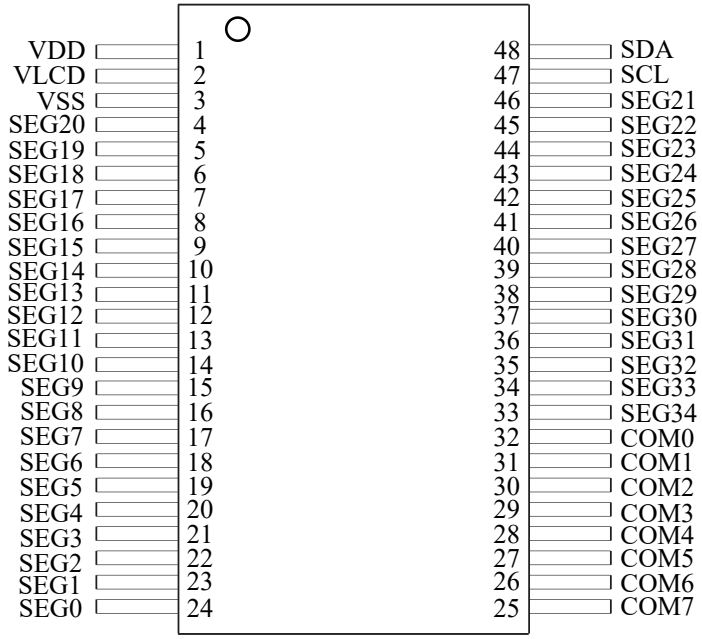
| Part No. | SEG/COM | Display points | Packaging |
|---|---|---|---|
| VKL060 | 15×4 | 60 | SSOP24 |
| VKL076 | 19×4 | 76 | SSOP28 |
| VKL092Q | 23×4 | 92 | QFN32L |
| VKL128 | 32×4 | 128 | LQFP44 |
| VKL144A | 36×4 | 144 | TSSOP48 |
| VKL144B | 36×4 | 144 | QFN48L |
| VKL144C | 36×4 | 144 | LQFP48 |
| VKL280 | 35×8 | 280 | TSSOP48/LQFP48 |

## 5 Ordering Information

| Part No. | Packaging | Tube Qty | Tray(reel) Qty | Box Qty | Total Qty | Notes |
|---|---|---|---|---|---|---|
| VKL060 | SSOP24 | 50/tube | | 10000/box | 100000 PCS | |
| VKL076 | SSOP28 | 50/tube | | 10000/box | 100000 PCS | |
| VKL092Q | QFN32L | | | 3000/box | 24000 PCS | |
| VKL128 | LQFP44 | | | 1600/box | 9600 PCS | |
| VKL144A | TSSOP48 | | 2000/reel | | 16000 PCS | |
| VKL144B | QFN48L | | 3000/reel | | 24000 PCS | |
| VKL144C | LQFP48 | | 250/tray | 2500/box | 15000 PCS | |
| VKL280 | TSSOP48 | | 2000/reel | | 16000 PCS | |
| | LQFP48 | | 250/tray | 2500/box | 15000 PCS | |

# 6 Package Pinout Information(TSSOP48)

TOP VIEW



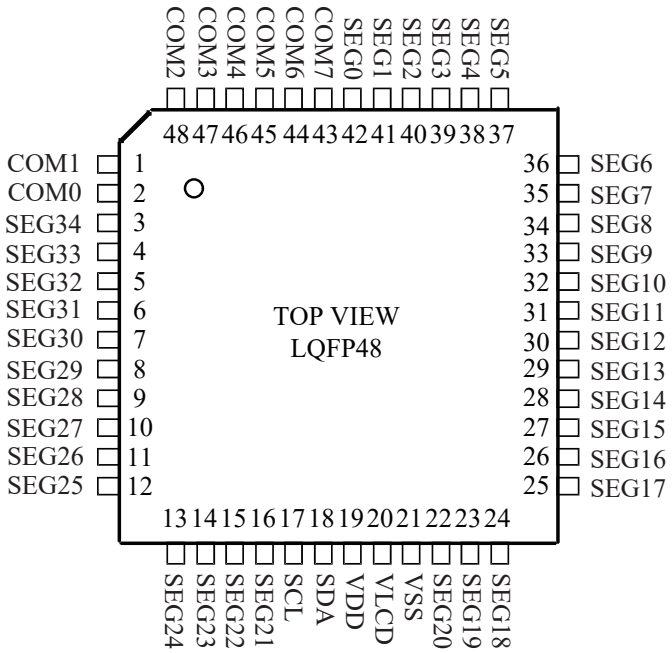

TSSOP48

For more information: Page 20

## 6.1 VKL280/TSSOP48 Pin Description

| No. | Name | I/O | Function |
|---|---|---|---|
| 4-24/ 46-33 | SEG20-SEG0/ SEG21-SEG34 | O | LCD SEG drive outputs |
| 32-25 | COM0-COM7 | O | LCD COM drive outputs |
| 2 | VLCD | I | LCD driving voltage |
| 1 | VDD | VDD | Positive power supply |
| 3 | VSS | VSS | Negative power supply |
| 47 | SCL | I | Serial Clock Input for I2C interface |
| 48 | SDA | I/O | Serial Data Input/Output for I2C interface |

# 7 Package Pinout Information(LQFP48)



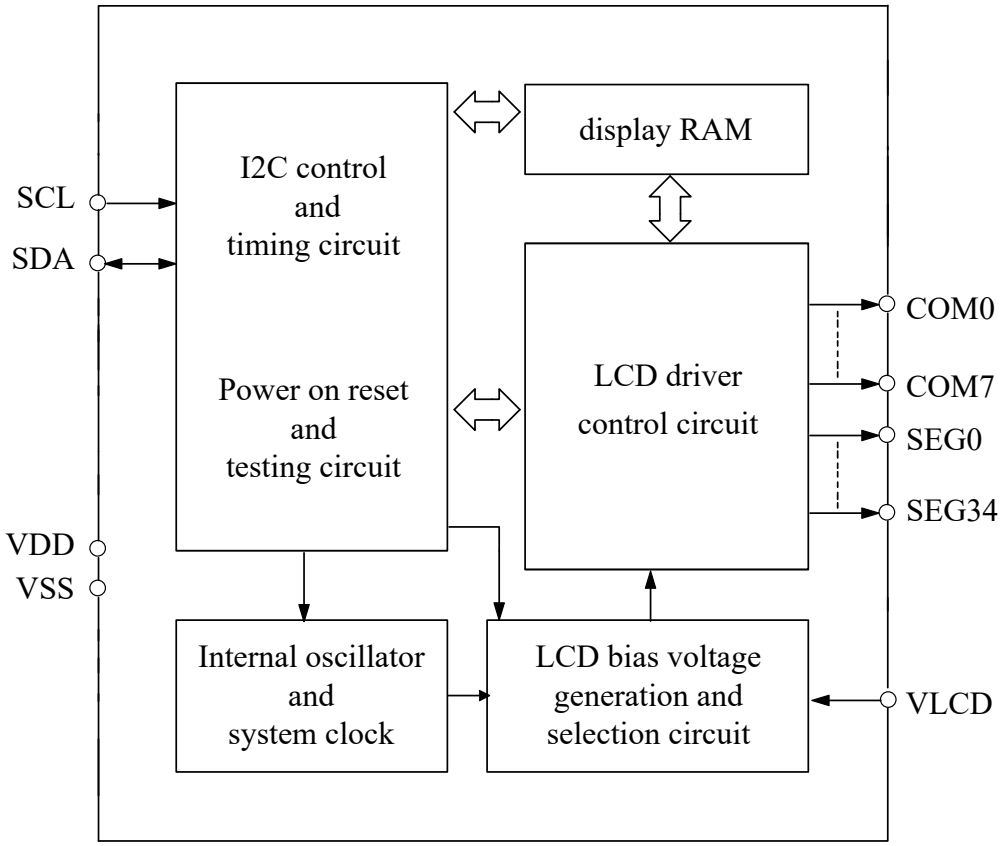

For more information: Page 21

## 7.1 VKL280/LQFP48 Pin Description

| No. | Name | I/O | Function |
|---|---|---|---|
| 42-22/ 16-3 | SEG0-SEG20/ SEG21-SEG34 | O | LCD SEG drive outputs |
| 1/2/ 48-43 | COM0-COM7 | O | LCD COM drive outputs |
| 20 | VLCD | I | LCD driving voltage |
| 19 | VDD | VDD | Positive power supply |
| 21 | VSS | VSS | Negative power supply |
| 17 | SCL | I | Serial Clock Input for I2C interface |
| 18 | SDA | I/O | Serial Data Input/Output for I2C interface |

# 8 Functional Description

## 8.1 Block Diagram



## 8.2 Function Description

1. Functional circuits

The VKL280 integrates all the necessary functional circuits for the LCD driver. These circuits include: LCD bias voltage generator, LCD voltage selector, internal clock (OSC = 25.6KHz), display register, SEG/COM output circuit, I2C serial interface, power-on reset circuit and display control circuit.

2. Display driving principle

The VKL280 can drive a maximum of 280 points (35 SEG × 8 COM) LCD screen. SEG0-SEG34 and COM0-COM7 are directly connected to the LCD. When used in applications with fewer than 35 SEG, the unused pins can be left unconnected. The VKL280 adopts a 1/8Duty, 1/4Bias driving method.

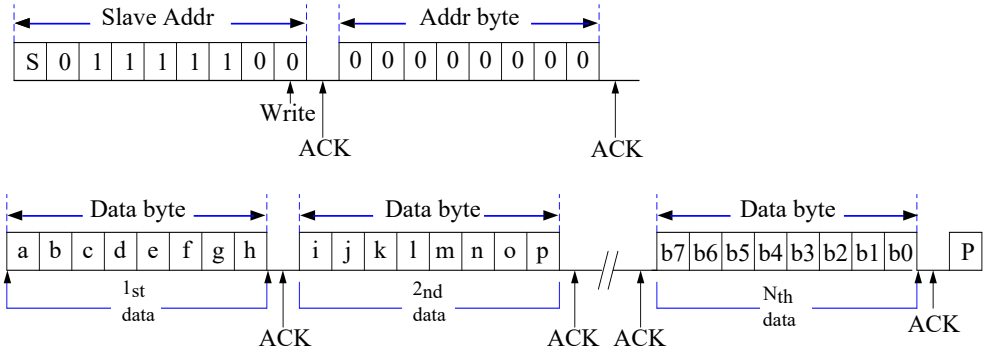
## 8.3 Display RAM

Static display memory (RAM) structure of 35 x 8 bits (35 seg x 8 com), the stored data. Display the contents of the RAM directly map into a LCD display content of the drive. I2C command access display RAM data, every read and write 4bit display data address automatically added 1.

Display the contents of the RAM mapping to LCD process shown in the table below:

| Output | COM7 | COM6 | COM5 | COM4 | COM3 | COM2 | COM1 | COM0 | Address |
|---|---|---|---|---|---|---|---|---|---|
| SEG0 | h | g | f | e | d | c | b | a | 0x00 |
| SEG1 | p | o | n | m | l | k | j | i | 0x01 |
| SEG2 | | | | | | | | | 0x02 |
| SEG3 | | | | | | | | | 0x03 |
| SEG4 | | | | | | | | | 0x04 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ |
| SEG33 | | | | | | | | | 0x21 |
| SEG34 | | | | | | | | | 0x22 |
| Display data | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | |

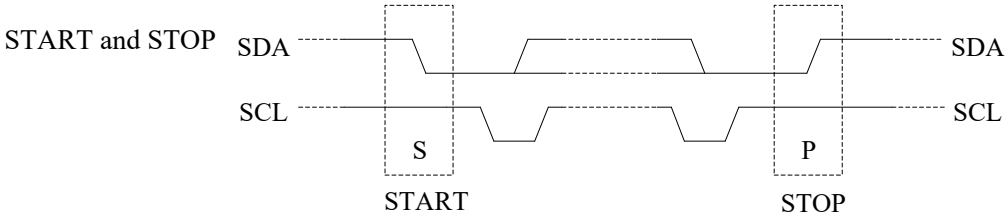
Note: the above data SEG0 - SEG3 and write data display RAM a - p corresponding relation is shown below:

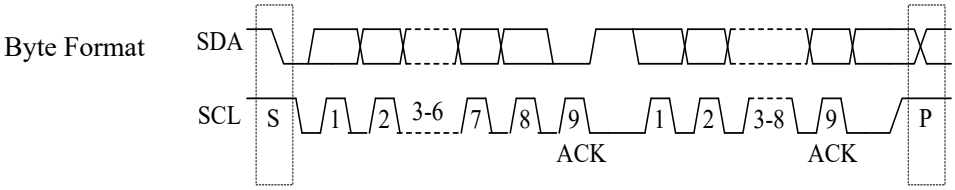


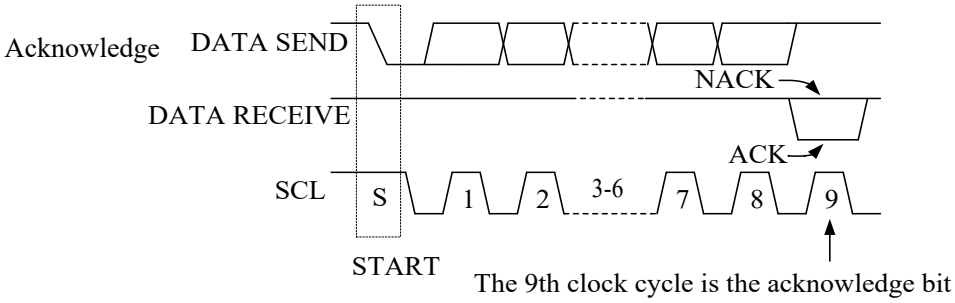
## 8.4 I2C Serial Interface

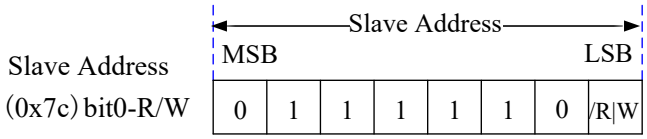
The VKL280 communicates via two I2C-compatible pins:SCL and SDA. These open-drain pins require external pull-up resistors.

The SCL pin is the clock input pin, and the SDA pin is the serial data input/output pin. Both SCL and SDA remain at logic high level when the I2C bus is idle.

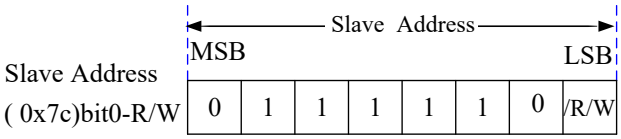


## 8.5 Command Summary




Bit7 determines the following byte type:0=Data(D), 1= Command(C)

## 8.6 Address set command

Set the working mode:

| Function | Byte | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address pointer | 1 | C/D | 0 | A5 | A4 | A3 | A2 | A1 | A0 | | W | |

| Bit5-0 | Address(bit6) |
|---|---|
| 000000 | 0x00 (Def) |
| 000001 | 0x01 |
| 000002 | 0x02 |
| ..... | ..... |
| 011111 | 0x1f |
| 100000 | 0x20 |
| 100001 | 0x21 |
| 100010 | 0x22 |

This register is used to set the starting address of the data before writing data, or to set the address for reading data/commands before reading data/commands.

Read and write data address range is 00 ~ 22 h, beyond which is set to 00 h; when reading commands, the address can be set to 23H/24H.

## 8.7 EVR Setting Command

| Function | Byte | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| Address pointer | 1 | C/D | 1 | 0 | EV4 | EV3 | EV2 | EV1 | EV0 |

EVR command can be set up 32 kinds of voltage is used to adjust the LCD drive voltage, drive circuit of electric pressure Vo and highest external power supply voltage VLCD relationships shown in the table below, need to meet the following two conditions at the same time, otherwise may lead to IC driver output voltage instability (the red part of it is prohibited to use) :

1.The VO voltage set by the EVR adjustment must be greater than 2.5V;

2.The EVR adjustment settings must ensure that the condition "VLCD-VO > 0.3" is met;

| EVR | Calculation formula | VLCD=5.500 | VLCD=5.000 | VLCD=4.000 | VLCD=3.500 | VLCD=3.000 | VLCD=2.500 | Unit |
|---|---|---|---|---|---|---|---|---|
| 0 | VLCD | VO=5.500 | VO=5.000 | VO=4.000 | VO=3.500 | VO=3.000 | VO=2.500 | V |
| 1 | 0.967*VLCD | VO=5.323 | VO=4.839 | VO=3.871 | VO=3.387 | VO=2.903 | VO=2.419 | V |
| 2 | 0.937*VLCD | VO=5.156 | VO=4.688 | VO=3.750 | VO=3.281 | VO=2.813 | VO=2.344 | V |
| 3 | 0.909*VLCD | VO=5.000 | VO=4.545 | VO=3.636 | VO=3.182 | VO=2.727 | VO=2.273 | V |
| 4 | 0.882*VLCD | VO=4.853 | VO=4.412 | VO=3.529 | VO=3.088 | VO=2.647 | VO=2.206 | V |
| 5 | 0.857*VLCD | VO=4.714 | VO=4.268 | VO=3.429 | VO=3.000 | VO=2.571 | VO=2.143 | V |
| 6 | 0.833*VLCD | VO=4.583 | VO=4.167 | VO=3.333 | VO=2.917 | VO=2.500 | VO=2.083 | V |
| 7 | 0.810*VLCD | VO=4.459 | VO=4.054 | VO=3.243 | VO=2.838 | VO=2.432 | VO=2.027 | V |
| 8 | 0.789*VLCD | VO=4.342 | VO=3.947 | VO=3.158 | VO=2.763 | VO=2.368 | VO=1.974 | V |
| 9 | 0.769*VLCD | VO=4.231 | VO=3.846 | VO=3.077 | VO=2.692 | VO=2.308 | VO=1.923 | V |
| 10 | 0.750*VLCD | VO=4.125 | VO=3.750 | VO=3.000 | VO=2.625 | VO=2.250 | VO=1.875 | V |
| 11 | 0.731*VLCD | VO=4.024 | VO=3.659 | VO=2.927 | VO=2.561 | VO=2.195 | VO=1.829 | V |
| 12 | 0.714*VLCD | VO=3.929 | VO=3.571 | VO=2.857 | VO=2.500 | VO=2.143 | VO=1.786 | V |
| 13 | 0.697*VLCD | VO=3.837 | VO=3.488 | VO=2.791 | VO=2.442 | VO=2.093 | VO=1.744 | V |
| 14 | 0.681*VLCD | VO=3.750 | VO=3.409 | VO=2.727 | VO=2.386 | VO=2.045 | VO=1.705 | V |
| 15 | 0.666*VLCD | VO=3.667 | VO=3.333 | VO=2.667 | VO=2.333 | VO=2.000 | VO=1.667 | V |
| 16 | 0.652*VLCD | VO=3.587 | VO=3.261 | VO=2.609 | VO=2.283 | VO=1.957 | VO=1.630 | V |
| 17 | 0.638*VLCD | VO=3.511 | VO=3.191 | VO=2.553 | VO=2.234 | VO=1.915 | VO=1.596 | V |
| 18 | 0.625"VLCD | VO=3.438 | VO=3.125 | VO=2.500 | VO=2.188 | VO=1.875 | VO=1.563 | V |
| 19 | 0.612*VLCD | VO=3.367 | VO=3.061 | VO=2.449 | VO=2.143 | VO=1.837 | VO=1.531 | V |
| 20 | 0.600*VLCD | VO=3.300 | VO=3.000 | VO=2.400 | VO=2.100 | VO=1.800 | VO=1.500 | V |
| 21 | 0.588*VLCD | VO=3.235 | VO=2.941 | VO=2.353 | VO=2.059 | VO=1.765 | VO=1.471 | V |
| 22 | 0.576"VLCD | VO=3.173 | VO=2.885 | VO=2.308 | VO=2.019 | VO=1.731 | VO=1.443 | V |
| 23 | 0.566*VLCD | VO=3.113 | VO=2.830 | VO=2.264 | VO=1.981 | VO=1.698 | VO=1.415 | V |
| 24 | 0.555*VLCD | VO=3.056 | VO=2.778 | VO=2.222 | VO=1.944 | VO=1.667 | VO=1.389 | V |
| 25 | 0.545*VLCD | VO=3.000 | VO=2.727 | VO=2.182 | VO=1.909 | VO=1.636 | VO=1.364 | V |
| 26 | 0.535*VLCD | VO=2.946 | VO=2.679 | VO=2.143 | VO=1.875 | VO=1.607 | VO=1.339 | V |
| 27 | 0.526*VLCD | VO=2.895 | VO=2.632 | VO=2.105 | VO=1.842 | VO=1.579 | VO=1.316 | V |
| 28 | 0.517*VLCD | VO=2.845 | VO=2.586 | VO=2.069 | VO=1.810 | VO=1.552 | VO=1.293 | V |
| 29 | 0.508*VLCD | VO=2.797 | VO=2.542 | VO=2.034 | VO=1.780 | VO=1.525 | VO=1.271 | V |
| 30 | 0.500*VLCD | VO=2.797 | VO=2.500 | VO=2.000 | VO=1.750 | VO=1.500 | VO=1.250 | V |
| 31 | 0.491*VLCD | VO=2.705 | VO=2.459 | VO=1.967 | VO=1.721 | VO=1.475 | VO=1.230 | V |

## 8.8 Display control command

Set the LCD driving mode, frame rate frequency and four power consumption modes

| Function | Byte | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Display control settings | 1 | C/D | 1 | 1 | 0 | FR1 | FR0 | SR1 | SR0 | | W | |

| Bit 4 | Bit 3 | Frame rate |
|---|---|---|
| FR1 | FR0 | |
| 0 | 0 | 80Hz(Def) |
| 0 | 1 | 71Hz |
| 1 | 0 | 64Hz |
| 1 | 1 | 53Hz |

| Bit1 | Bit0 | Power consumption mode |
|---|---|---|
| SR1 | SR0 | |
| 0 | 0 | Power-saving Mode 1(LP1) |
| 0 | 1 | Power-saving Mode 2(LP2) |
| 1 | 0 | Normal mode (NP)(Def) |
| 1 | 1 | High power mode(HP) |

## 8.9 System Settings Command

Set system parameters:

| Function | Byte | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address pointer | 1 | C/D | 1 | 1 | 1 | 0 | Mode | R | DSP | | W | |

| Bit2 | Chip settings |
|---|---|
| DM | |
| 0 | line Flip |
| 1 | frame Flip(Def) |

| Bit1 | Software reset |
|---|---|
| R | |
| 0 | No operation(Def) |
| 1 | Software reset |

| Bit0 | Display screen on /off control |
|---|---|
| DSP | |
| 0 | Display off(Def) |
| 1 | Display on |

## 8.10 Full Pixel Control Command

| Function | Byte | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 | Note | R/W | Def |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address pointer | | C | 1 | 1 | 1 | 1 | 0 | Apon | Apoff | | | |

| Bit1 Apon | Enable control for all pixels |
|---|---|
| 0 | Normal(Def) |
| 1 | All pixels are activated. |

| Bit0 Apoff | All pixel disabling control |
|---|---|
| 0 | Normal(Def) |
| 1 | All pixels are turned off. |

Full bright full dark control, the register only when display works;
When both Apon and Apoff are 1, the display is fully dark, meaning that Apoff has a higher priority than Apon.

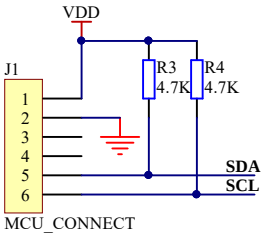
## 8.11 Work process

| No. | 输入 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 描述 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 开启电源 | | | | | | | | | VDD =0→5V（上升时间0.1ms) |
| | ↓ | | | | | | | | | |
| 2 | 等待 100us | | | | | | | | | 初始化 IC |
| | ↓ | | | | | | | | | |
| 3 | 停止 | | | | | | | | | 发送停止条件 |
| | ↓ | | | | | | | | | |
| 4 | 开始 | | | | | | | | | 发送起始条件 |
| 5 | 从设备地址 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 发送从机地址（0x7C） |
| | ↓ | | | | | | | | | |
| 6 | ICSET | 1 | 1 | 1 | 1 | 0 | * | 1 | * | 软件复位 |
| | ↓ | | | | | | | | | |
| 7 | DISCTL | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 初始值设置时可不执行 |
| | ↓ | | | | | | | | | （如需更改条件则执行） |
| 8 | EVRSET | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 初始值设置时可不执行 |
| | ↓ | | | | | | | | | （如需更改条件则执行） |
| 9 | ADSET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 设置RAM 地址 |
| | ↓ | | | | | | | | | |
| 10 | 显示数据 | * | * | * | * | * | * | * | * | 地址00h 的数据 |
| | ⋮ | | | | | | | | | 连续写入数据... |
| | 显示数据 | * | * | * | * | * | * | * | * | 地址 22h 的数据 |
| | ↓ | | | | | | | | | |
| 11 | 停止 | | | | | | | | | 发送停止条件 |
| | ↓ | | | | | | | | | |
| 12 | 开始 | | | | | | | | | 发送起始条件 |
| 13 | 从设备地址 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 发送从设备地址(01111100) |
| | ↓ | | | | | | | | | |
| 14 | ICSET | 1 | 1 | 1 | 1 | 0 | * | 0 | 1 | 显示开启 |

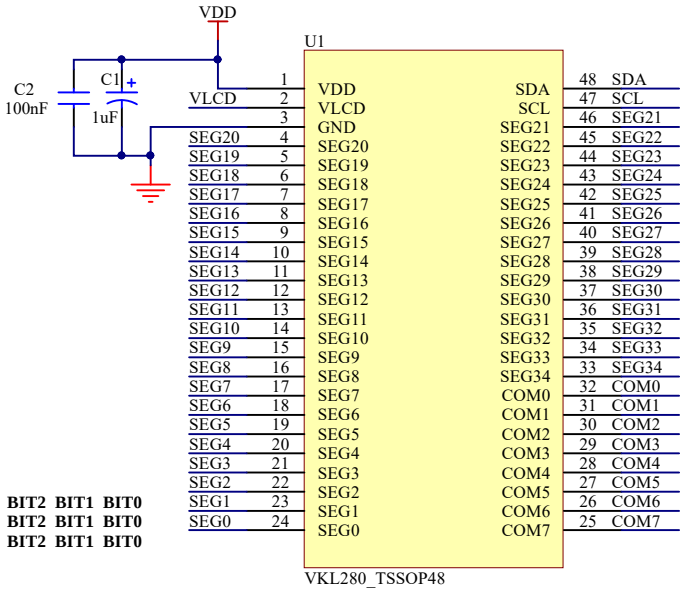
# 9 Application Circuits/TSSOP48

When there is a lot of external interference, a 10R to 1k resistor and a pF-level ground capacitor can be connected in series to the communication pin. When the power supply voltages of the single-chip microcontroller (3.3V) and the driver chip (5V) are inconsistent, it is recommended to add a level conversion circuit to the communication pin.

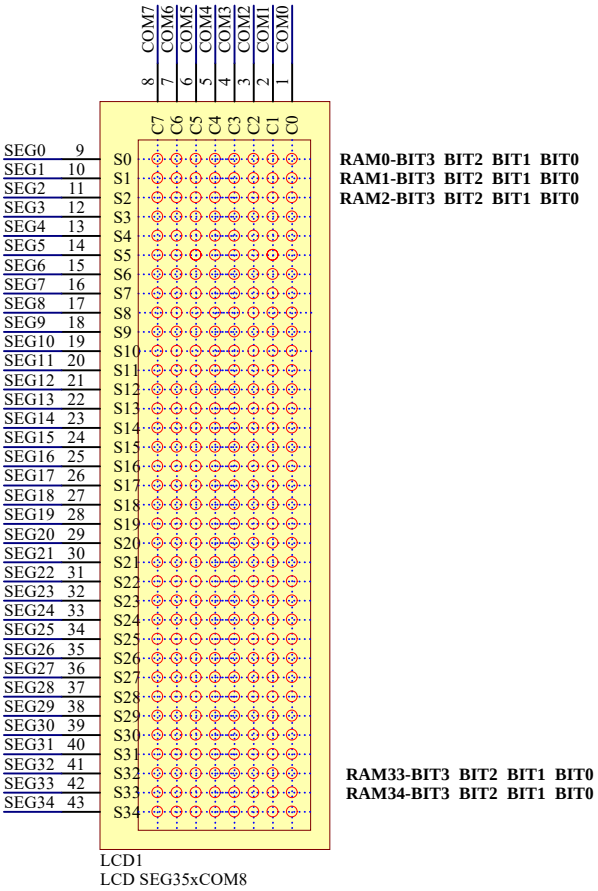
**VDD=2.5V-5.5V**




VLCD pin external 2.5-5.5V power supply, can not be suspended



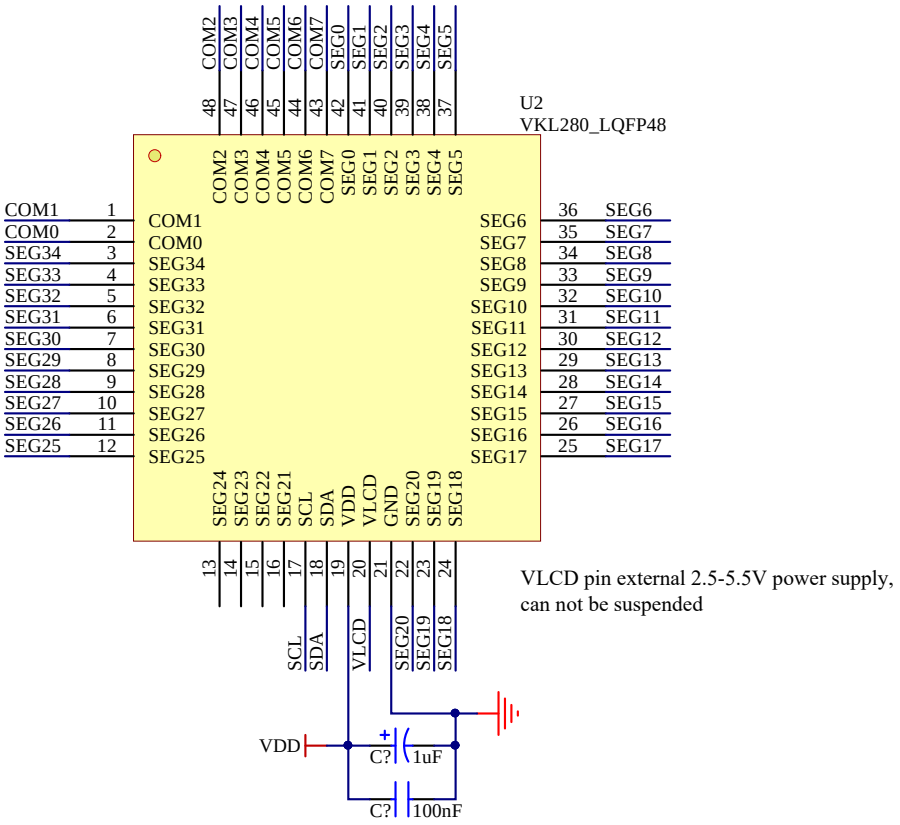

It is recommended that the COM pins of the chip and the COM pins of the LCD be connected in a 1-to-1 manner to the SEG pins. For the convenience of PCB routing, the connection order can be changed.
Please note that when writing the software, the corresponding order of the display RAM also needs to be adjusted.




**RAM0-BIT3 BIT2 BIT1 BIT0**
**RAM1-BIT3 BIT2 BIT1 BIT0**
**RAM2-BIT3 BIT2 BIT1 BIT0**

**RAM33-BIT3 BIT2 BIT1 BIT0**
**RAM34-BIT3 BIT2 BIT1 BIT0**

## 9.1 Application Circuits/LQFP48



# 10 Electrical Characteristics

## 10.1 Absolute Maximum Ratings

| 特性 | 符号 | 极限值 | 单位 |
|---|---|---|---|
| 电源电压 | VDD | -0.5~+6.5 | V |
| 液晶工作电压 | VLCD | -0.5~+6.5 | V |
| 输入电压SDA、SCL | Vi | Vss-0.5~Vdd+0.5 | V |
| 输出电压SEG、COM | Vo | V1cd-0.5~V1cd+0.5 | V |
| VDD, VSS, VLCD 电流 | VDD, VSS, VLCD | -50~+50 | mA |
| 最大功耗 | Ptot | 400 | mA |
| 工作温度 | Topr | -40~ +85 | ℃ |
| 贮存温度 | Tstg | -65~ +150 | ℃ |

## 10.2 DC Electrical Characteristics

(VDD=2. 5V~5. 5V, VLCD=2. 5V~5.5V, VSS=0, Ta=-40~85°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Operating voltage | VDD | 2.5 | — | 5.5 | V | — |
| LCD working voltage | VLCD | 2.5 | — | 5.5 | V | — |
| Sleep current | IST | — | — | 0.5 | μA | Turn off the display, turn off the internal oscillator |
| Working current | IDD | — | 2 | 5 | μA | VDD=3.3V, VLCD=5V, T=25°C, Energy-saving mode, frequency 80, 1/4 bias, frame inversion |
| LCD working current | ILCD | — | 6 | 10 | μA | VDD=3.3V, VLCD=5V, T=25°C, Energy-saving mode, frequency 80, 1/4 bias, frame inversion |
| Frame frequency | FCLK | 60 | 80 | 110 | Hz | VDD=3. 3V, FR=80Hz |
| Dc component | $V_{CM}$ | -20 | — | +20 | mV | VCM=32 nF, COM0~COM7 |
| | $V_S$ | -20 | — | +20 | mV | VS=4. 7 nF, SEG0~SGE34 |
| I2C high-level voltage | $V_{IH}$ | 0.6VDD | — | VDD | V | SDA, SCL |
| I2C low voltage level | $V_{IL}$ | VSS | — | 0.3VDD | V | SDA, SCL |
| I2C high-level current | $I_{IH}$ | — | — | 1 | μA | SDA, SCL |
| I2C low-level current | $I_{IL}$ | -1 | — | — | μA | SDA, SCL |
| LCD driving impedance | $R_{ON}$ | — | 3.5 | — | kΩ | SEG Iload=±10μA |
| | $R_{ON}$ | — | 3.5 | — | kΩ | COM Iload=+10μA |

NOTE: The supply voltage for the DC component is (VDD=3.3V, VLCD=5V), EVR=8, Ta=25 °C

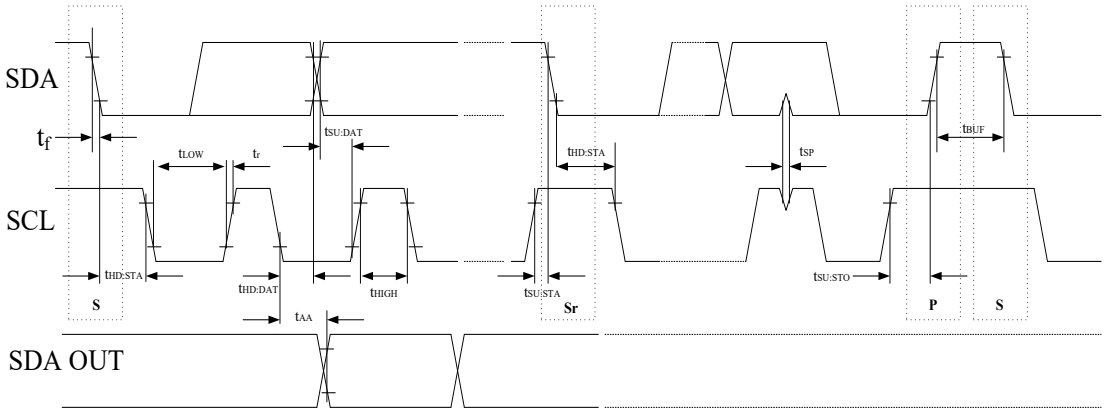
## 10.3 Electromagnetic Parameters and Humidity Sensitivity Grade

| Project | Level | Testing standards |
|---|---|---|
| ESD(HBM) | ±8kKV | JESD22-A114F |
| Latch-up | ±100mA | JESD78A |
| MSL | 3 | JEDEC |

I2C Parameters

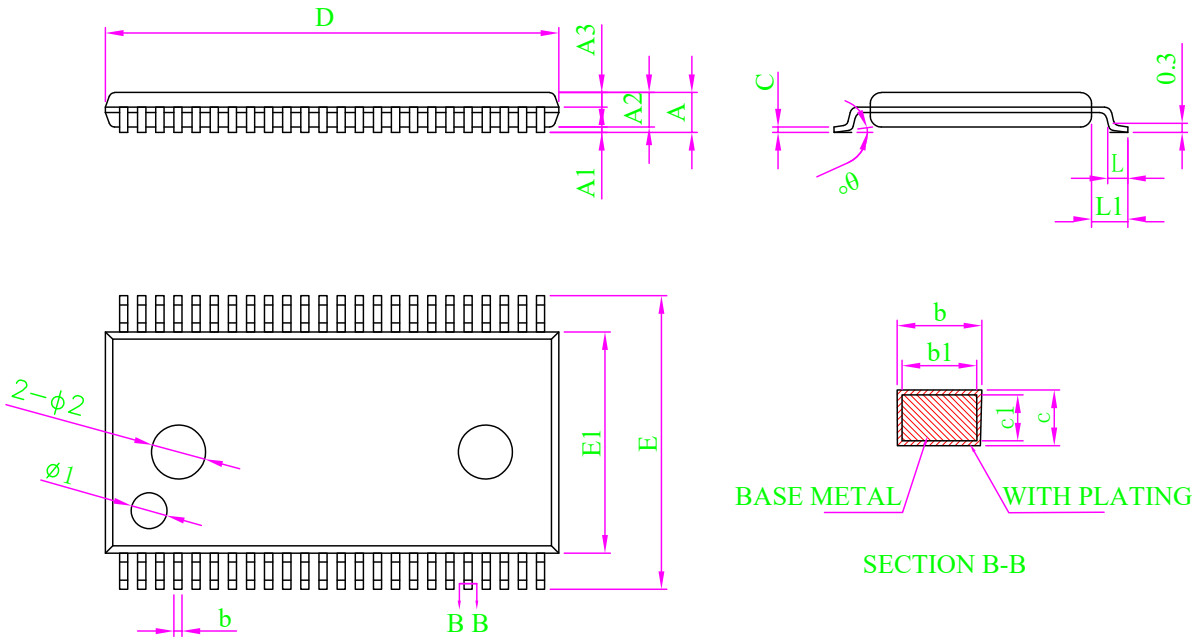
| Name | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Input rise time | tr | — | — | 0.3 | μs |
| Input deceleration time | tf | — | — | 0.3 | μs |
| SCL Turnaround Time | $t_{SCYC}$ | 2.4 | — | — | μs |
| “H”SCL pulse width | $t_{SHw}$ | 0.6 | — | — | μs |
| “L”SCL pulse width | $t_{SLW}$ | 1.2 | — | — | μs |
| SDA Set the time | $t_{SDS}$ | 100 | — | — | ns |
| SDA Maintain time | $t_{SDH}$ | 100 | — | — | ns |
| Bus idle time | $t_{BUF}$ | 1.3 | — | — | μs |
| Start-up condition holding time | $t_{HD;STA}$ | 0.6 | — | — | μs |
| Startup condition setting time | $t_{SU;STA}$ | 0.6 | — | — | μs |
| Stop condition setting time | $t_{SU;STO}$ | 0.6 | — | — | μs |

## $I^2C$ Timing


SDA
SCL
SDA OUT
tf
tLOW
tr
tSU:DAT
tHD:STA
tSP
tBUF
tHD:STA
tHD:DAT
tHIGH
tSU:STA
tSU:STO
tAA
S
Sr
P
S

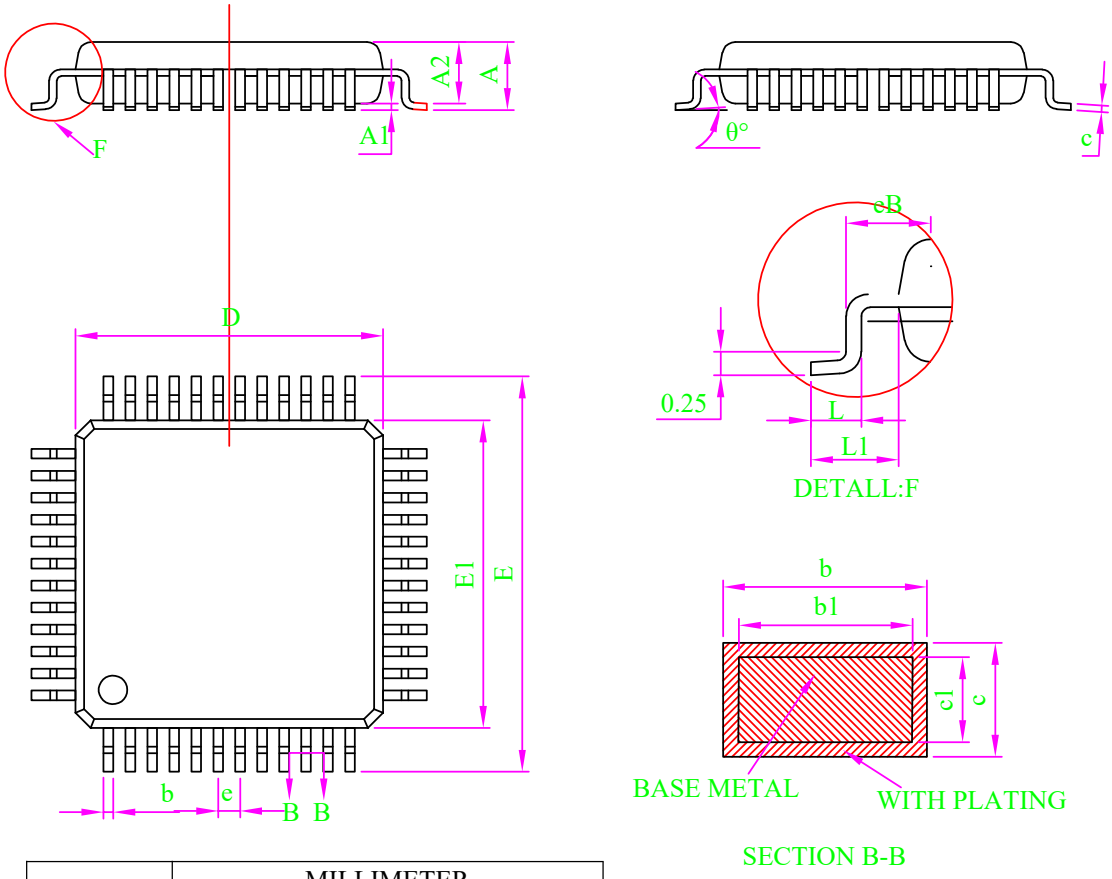
# 11 Package Information

## 11.1 TSSOP48(240mil)(12.5mm x 6.1mm PP=0.5mm)




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.20 |
| A1 | 0.05 | 0.10 | 0.15 |
| A2 | 0.85 | 0.95 | 1.05 |
| A3 | 0.35 | 0.40 | 0.45 |
| b | 0.19 | - | 0.28 |
| b1 | 0.18 | 0.20 | 0.23 |
| c | 0.15 | - | 0.21 |
| c1 | 0.14 | 0.15 | 0.16 |
| D | 12.40 | 12.50 | 12.60 |
| E | 7.90 | 8.10 | 8.30 |
| E1 | 6.00 | 6.10 | 6.20 |
| e | 0.50BSC | | |
| L | 0.45 | - | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | - | 8° |
| Φ1 | Φ1.00*0.10±0.05DP | | |
| Φ2 | Φ1.50*0.075±0.025DP | | |

## 11.2 LQFP48（7.0mm x 7.0mm PP=0.5mm）




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | - | 1.70 |
| A1 | 0.10 | 0.15 | 0.20 |
| A2 | 1.30 | 1.40 | 1.50 |
| b | 0.18 | - | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | - | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| eB | 8.10 | - | 8.28 |
| E1 | 6.90 | 7.00 | 7.10 |
| e | 0.50 BSC | | |
| L | 0.42 | 0.57 | 0.72 |
| L1 | 0.90 | 1.00 | 1.10 |
| θ | 0 | - | 10° |

Note:

1. All dimension are in mm.
2. Dim D&El does not include plastic flash； Flash: Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.007mm-0.015mm

# 12 Disclaimer

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# 13 Revision History

| No. | Version | Date | Modify the content | Check |
|---|---|---|---|---|
| 1 | 1.0 | 2018-08-10 | Initial release | YES |
| 2 | 1.1 | 2026-02-05 | Change Description | YES |
| | | | | |
| | | | | |

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/