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Vinka Microelectronics

VKL092Q Datasheet

23×4 LCD DRIVER

Rev.1.3

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1 General Description

The VKL092Q is a segment-type memory-mapped LCD driver that drive LCD screens with a maximum of 92 dots (23SEG×4COM). It can be configured via the I2C interface to set display parameters and access display data. It supports four selectable power modes and can also enter power-down mode by Display-OFF instruction. Its high noise immunity and ultra-low power consumption features make it suitable for water, electricity and gas meters as well as various industrial control instruments.

2 Key Features

- Operating voltage：2.5-5.5V
- Built-in RC oscillator (default)
- Selectable LCD bias:1/2、1/3
- Selectable LCD duty:1/4
- Built-in 23×4-bit display RAM
- The frame frequency can be configured as 80Hz or 71Hz、64Hz、53Hz
- Power-down mode via software command(LCD OFF)
- Supports four selectable power modes
- I2C communication interface
- Display mode 23×4
- Three display overall flicker frequencies
- Software-configurable LCD parameters
- Auto-increment addressing for sequential read/write
- VLCD pin provides LCD driving voltage(equal to VDD-VLCD)
- Built-in power-on reset circuit (POR)
- Low power consumption and high anti-interference
- Available Packages:
  QFN32L(4.0mm × 4.0mm PP=0.4mm)

3 Application field

- Panel watch
- Medical devices

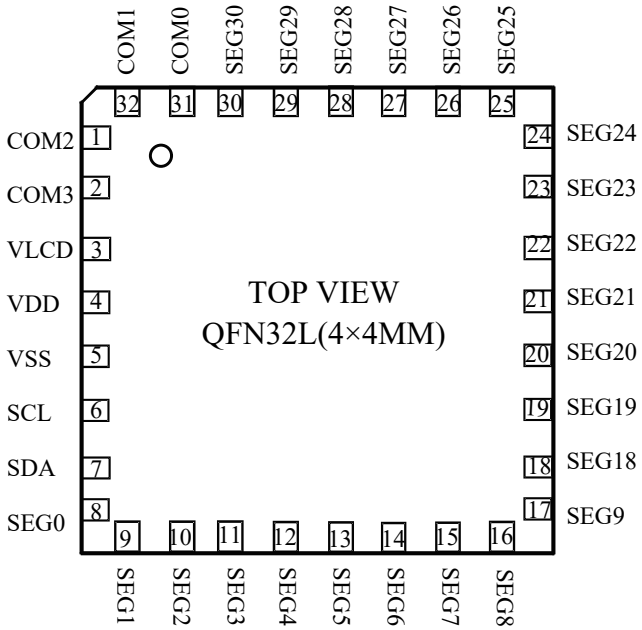
4 Product Selection

Part No.	SEG/COM	Display points	Packaging
VKL060	15×4	60	SSOP24
VKL076	19×4	76	SSOP28
VKL092Q	23×4	92	QFN32L
VKL128	32×4	128	LQFP44
VKL144A	36×4	144	TSSOP48
VKL144B	36×4	144	QFN48L
VKL144C	36×4	144	LQFP48
VKL280	35×8	280	TSSOP48/LQFP48

5 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel) Qty	Box Qty	Total Qty	Notes
VKL060	SSOP24	50/tube		10000/box	100000 PCS	
VKL076	SSOP28	50/tube		10000/box	100000 PCS	
VKL092Q	QFN32L			3000/box	24000 PCS	
VKL128	LQFP44			1600/box	9600 PCS	
VKL144A	TSSOP48		2000/reel		16000 PCS	
VKL144B	QFN48L		3000/reel		24000 PCS	
VKL144C	LQFP48		250/tray	2500/box	15000 PCS	
VKL280	TSSOP48		2000/reel		16000 PCS	
	LQFP48		250/tray	2500/box	15000 PCS	

6 Package Pinout Information(QFN32L)



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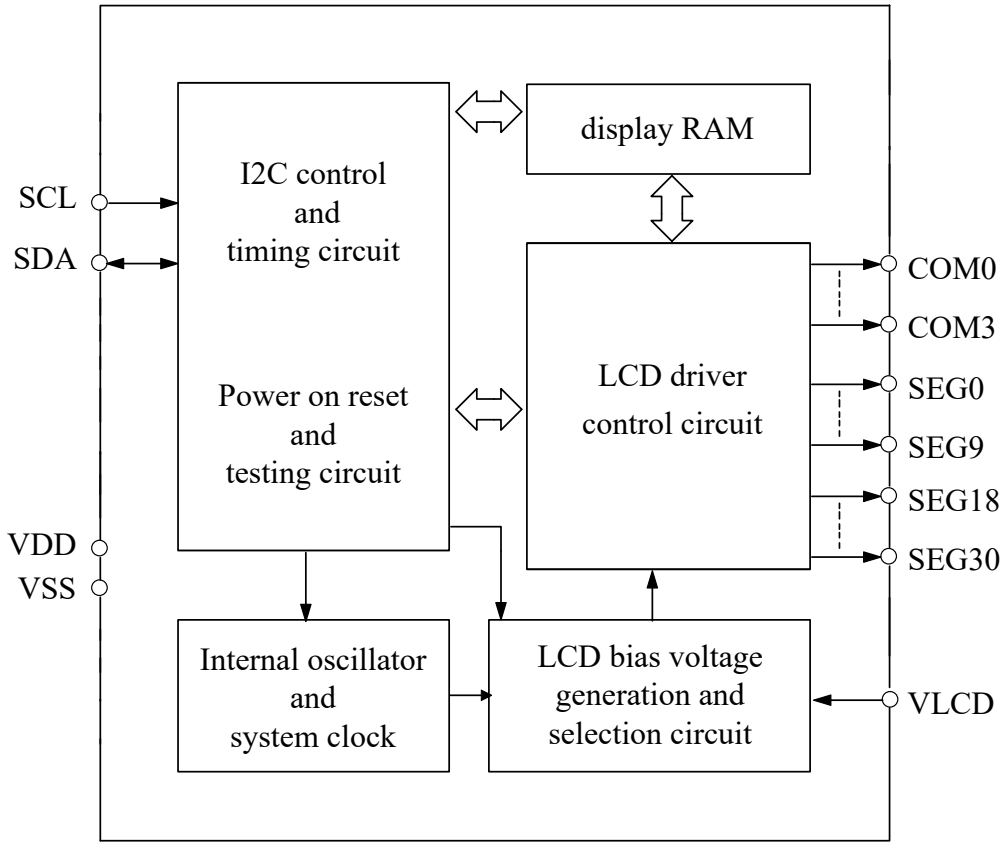
6.1 VKL092Q/QFN32L Pin Description

No.	Name	I/O	Function
31,32 1,2	COM0-COM3	O	LCD COM drive outputs
3	VLCD	I	LCD driving voltage (equal to VDD-VLCD)
4	VDD	VDD	Positive power supply
5	GND	GND	Negative power supply
6	SCL	I	Serial Clock Input for I2C interface
7	SDA	I/O	Serial Data Input/Output for I2C interface
8-17	SEG0-SEG9	O	LCD SEG drive outputs
18-30	SEG18-SEG30	O	LCD SEG drive outputs

7 Functional Description

7.1 Block Diagram



7.2 Display RAM

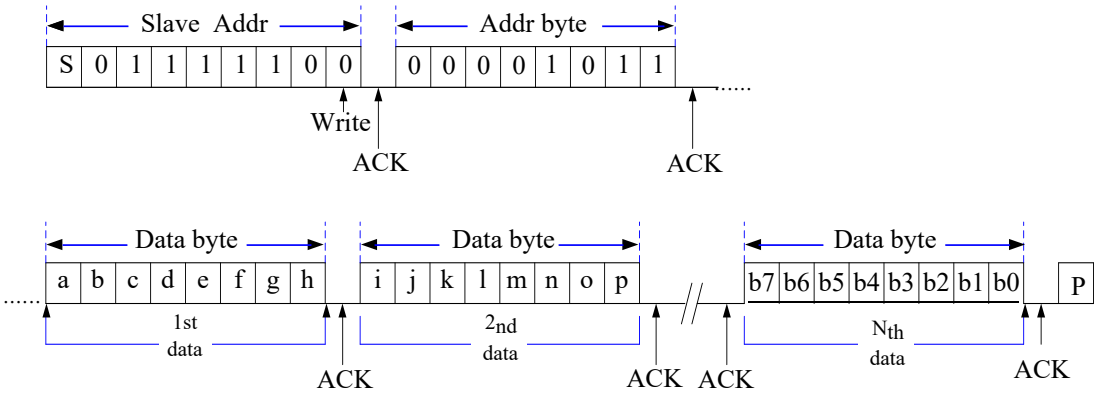
The display RAM is organized as 23×4 bits (23SEG×4COM), which stores the displayed data. The content of the display RAM is directly mapped to the display content of the LCD driver. Display RAM data is accessed via I2C commands. Address auto-increment each 4 bits data read/write.

The following is a mapping from the RAM to the LCD pattern:

Output	COM3	COM2	COM1	COM0	Address	Output	COM3	COM2	COM1	COM0	Address
SEG1	h	g	f	e	0x01	SEG0	d	c	b	a	0x00
SEG3	p	o	n	m	0x03	SEG2	l	k	j	i	0x02
SEG5					0x05	SEG4					0x04
SEG7					0x07	SEG6					0x06
SEG9					0x09	SEG8					0x08
SEG19					0x13	SEG18					0x12
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
						SEG30					0x1E
Data	bit7	bit6	bit5	bit4			bit3	bit2	bit1	bit0	

RAM Mapping of 23×4

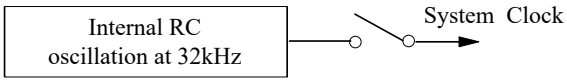
Example: The correspondence between data SEG9-SEG12 and data a-p written into the display RAM is shown in the following figure:



7.3 System Oscillator

The VKL092Q system clock generates LCD driving signals and internal timing. The system clock source comes from the internal RC oscillator（32kHz），System clock frequency(f_{SYS}) Determine the LCD frame rate。

The setting of the system clock is shown in the following figure:

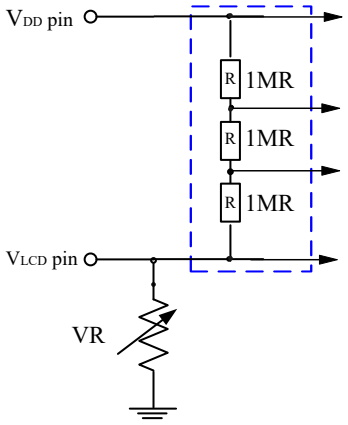


7.4 LCD driver voltage

LCD driving voltage (VLCD≤VDD) is generated via resistor from VLCD to VSS. The LCD driving voltage =VDD-VLCD. An internal operational amplifier is used to achieve low-power driving.

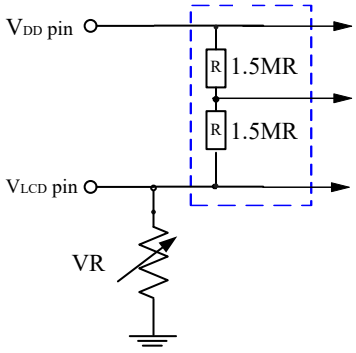
Use a 1MΩ variable resistor(VR) to adjust contrast, retain the resistance value after optimization.

1/3Bias



The resistance value is in the MΩ range and for reference only.

1/2Bias



The resistance value is in the MΩ range and for reference only.

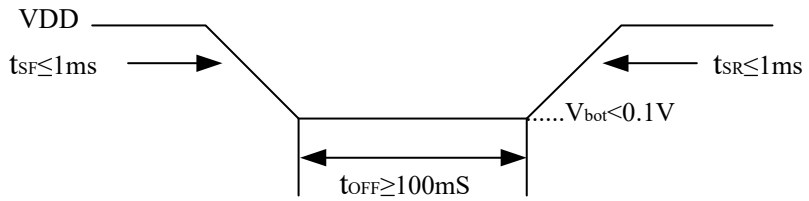
7.5 Power-On Reset

Do not initiate I2C communication during the 1mS power-on reset(POR) period.
The state of the internal circuit after initialization is as follows:

- When VLCD≤VDD, all COM/SEG pins output VDD level..
- 1/4 duty and 1/3 bias.
- The system oscillator and LCD bias generator are turned off.
- LCD display off.
- Blinking function prohibited.

When powered on, the POR circuit ensures normal RESET inside the circuit. During the operation of the chip, if the VDD drops below the specified minimum operating voltage, the power-on reset timing condition must be met, that is, the VDD voltage must drop to 0V and remain at 0V for at least 100ms before rising to the normal operating voltage

Power-on Reset Timing：



7.6 LCD Communication Command

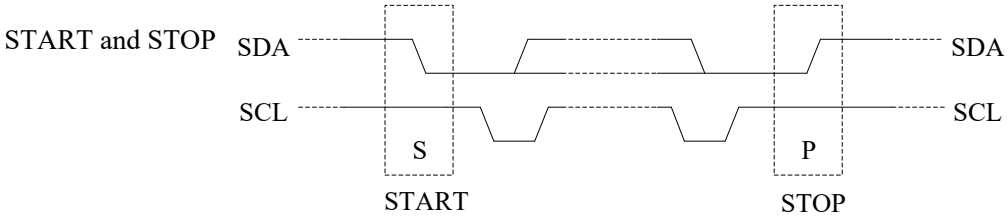
The display mode supported by the LCD driver is 23SEG×4COM, with unused SEG and COM pins suspended. The LCD frame frequency is software selectable: 80Hz(default),71Hz,64Hz,53Hz.

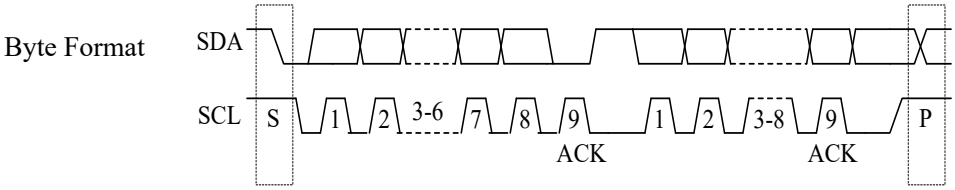
Display parameters and display data can be Configured and accessed through the I2C interface.

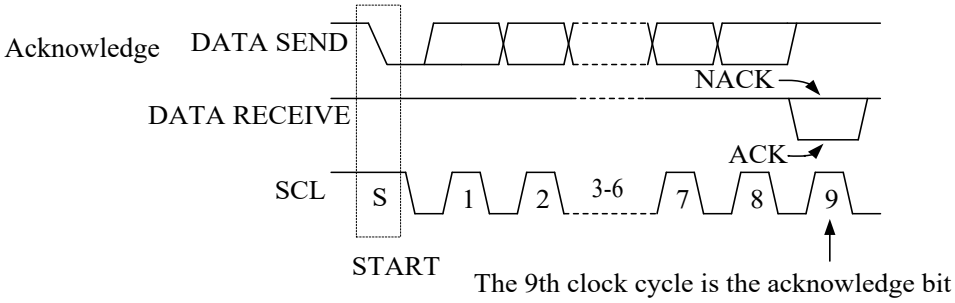
7.7 I2C Serial Interface

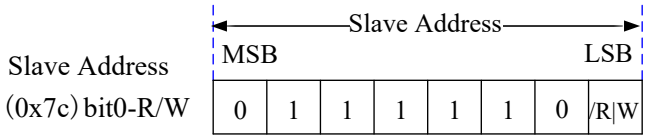
The VKL092Q communicates via two I2C-compatible pins:SCL and SDA. These open-drain pins require external pull-up resistors.

The SCL pin is the clock input pin, and the SDA pin is the serial data input/output pin. Both SCL and SDA remain at logic high level when the I2C bus is idle.





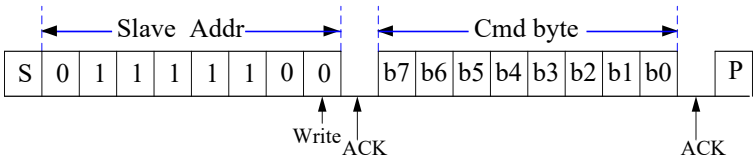




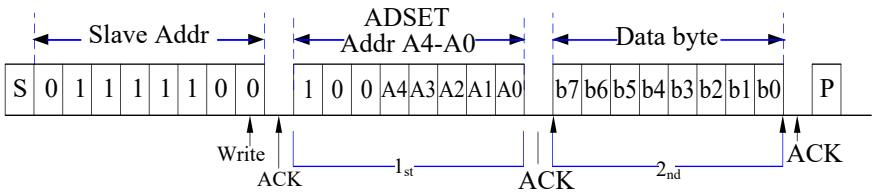
7.8 I2C Command Format

Write operation

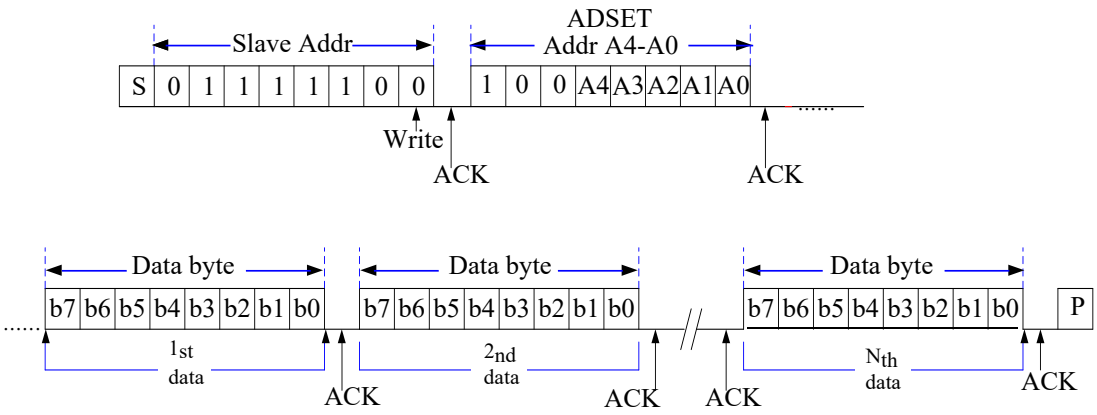
Write commands



Write a single byte to the display RAM

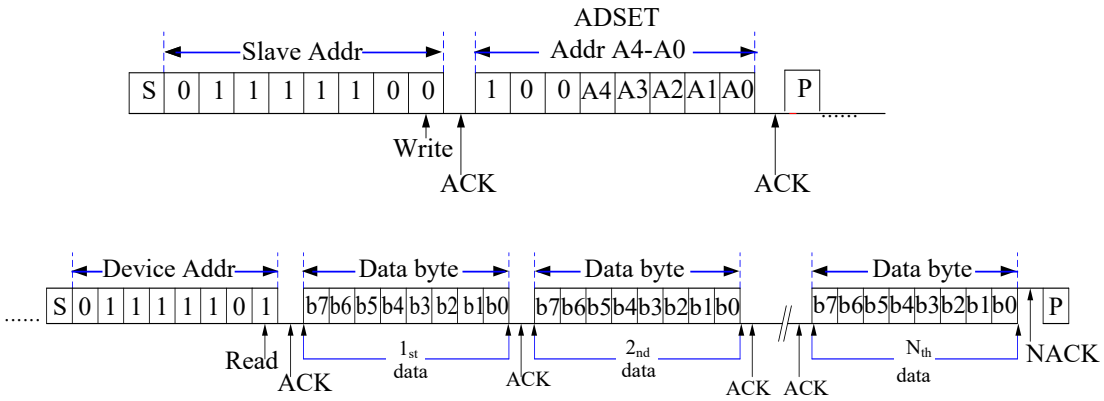


Write multiple bytes to the display RAM

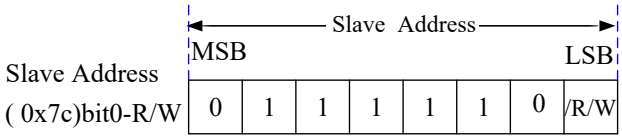


Read operation

Read multiple bytes from the display RAM



7.9 Command Summary



Bit7 determines the following byte type:0=Data(D), 1= Command(C)

7.10 Display Mode Command

Set Display mode:

Function	Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Note	R/W	Def
Address pointer	1	C/D	1	0	X	E	M0	X	X		W	

Bit3	LCD display
E	
0	OFF (Def)
1	ON

Bit2	LCD Bias
M0	
0	1/3 bias (Def)
1	1/2 bias

7.11 System Settings Commands

Set system parameters:

Function	Byte	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit 0	Note	R/W	Def
Address pointer	1	C/D	1	1	0	1	0	R	0		W	

Bit1	Soft reset
R	
0	Not Execute(Def)
1	Execute Soft reset

7.12 Address setting command

Set the start address for display RAM access

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Def
Address pointer	1	C/D	0	0	A4	A3	A2	A1	A0	W	

Bit4-0	Address(bit4-0)
A4-A0	
00000	0x00(Def)
01010	0x0A
01011	0x0B
.....	.....
11011	0x1E

7.13 All-pixel on/off command

Set the global pixel display state of the LCD:

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Address pointer	1	C/D	1	1	1	1	1	AP1	AP0		W	

Bit 1	Bit 0	All-pixel on/off control
AP1	AP0	
0	0	Normal(Def)
0	1	All-pixel off
1	0	All-pixel on
1	1	All-pixel off

Note: 1. This command does not alter display RAM contents

2. This command is effective only when LCD display on

7.14 Blinking frequency setting command

Set blinking frequency of the LCD

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
blinking frequency setting	1	C/D	1	1	1	0	0	BK1	BK0		W	

Bit 1	Bit 0	Blinking frequency
BK1	BK0	
0	0	Blinking off (Def)
0	1	0.5Hz
1	0	1Hz
1	1	2Hz

7.15 Display control command

Set LCD driver mode, frame frequency and four power modes

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Display control Settings	1	C/D	0	1	FR1	FR0	DM	SR1	SR0		W	

Bit 4	Bit 3	Frame frequency
FR1	FR0	
0	0	80Hz (Def)
0	1	71Hz
1	0	64Hz
1	1	53Hz

Bit2	Driving mode
DM	
0	Line inversion (Def)
1	Frame inversion

Bit1	Bit0	Power mode	Power consumption
SR1	SR0		
0	0	Lower Power mode 1 (LP1)	x0.5
0	1	Lower Power mode 2 (LP2)	0.67
1	0	Normal mode (NP)(Def)	1.0
1	1	High Performance mode(HP)	1.8

Operating current:

1.80 Hz 71 Hz > > 64 Hz > 53 Hz

2. Line inversion>Frame invers

3. High Performance mode > Normal Mode > Lower Power mode 2> Lower Power mod

4. Power consumption may vary depending on the LCD characteristics; values are reference only

Different display control commands have different display effects, as shown in the following table:

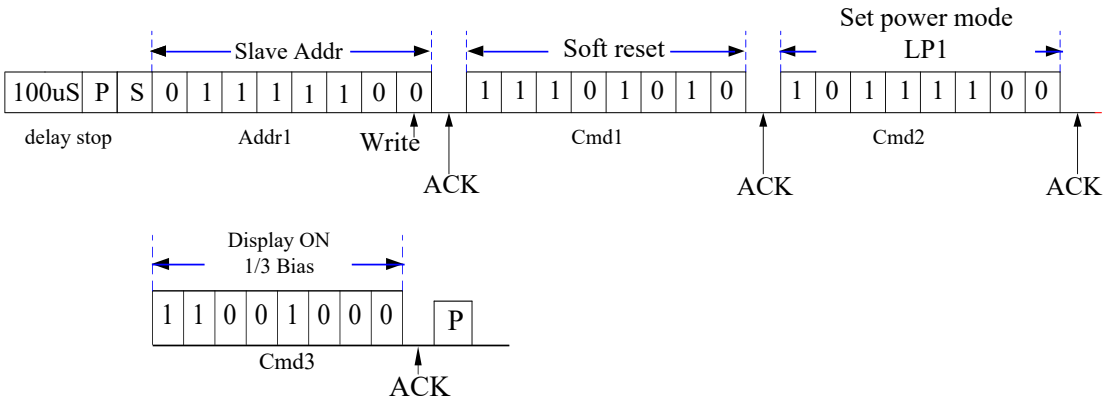
Display control	Visual stability	Display effect/contrast
Frame frequency	V	---
Driving mode	V	V
Power consumption mode	---	V
The impact is not absolute and is also related to the LCD used.		

8 Command Application

8.1 Initialize sequence

When powering on, the power-on reset sequence must be met. After power-on, parameters need to be configured first.

The initial parameters are configured through a series of commands, and the command sequence is as follows:



Power on: Ensure compliance POR timing requirements

Delay: Wait for the chip initialization with a delay of 100 microseconds

STOP: Send the I2C stop signal

START: Send the I2C start signal

Addr1: Send the Slave address (0x7c)

Cmd1: System Settings Command - Set Soft Reset (0xEA)

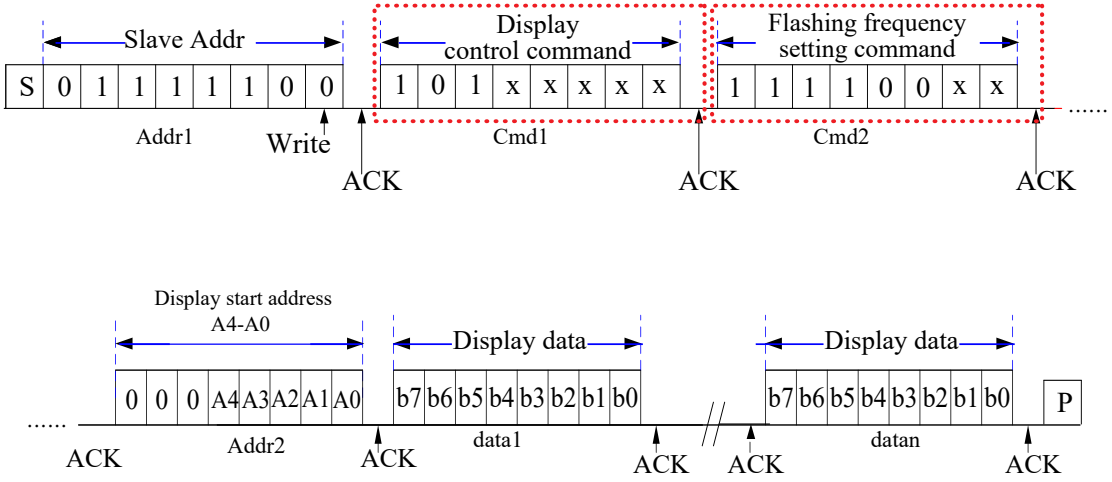
Cmd2: Data read, write, display and control commands - Set according to customer needs,
e.g,, Configure power mode: LP1(0xBC)
example, set to the most power-saving mode (0xBC)

Cmd3: Mode setting command - set Display state and Bias.
e.g,, Display ON and SET 1/3 BIAS (0xC8)

STOP: Send the I2C stop signal

8.2 Send display data

When the display control is initialized, it has been configured and there is no need to change the blinking configuration. Only the display data needs to be sent.



START: Send the I2C start signal

Addr1: Send the Slave address (0x7c)

Cmd1: Display control command - Set as needed. If the display control does not need to be changed, this byte does not have to be sent

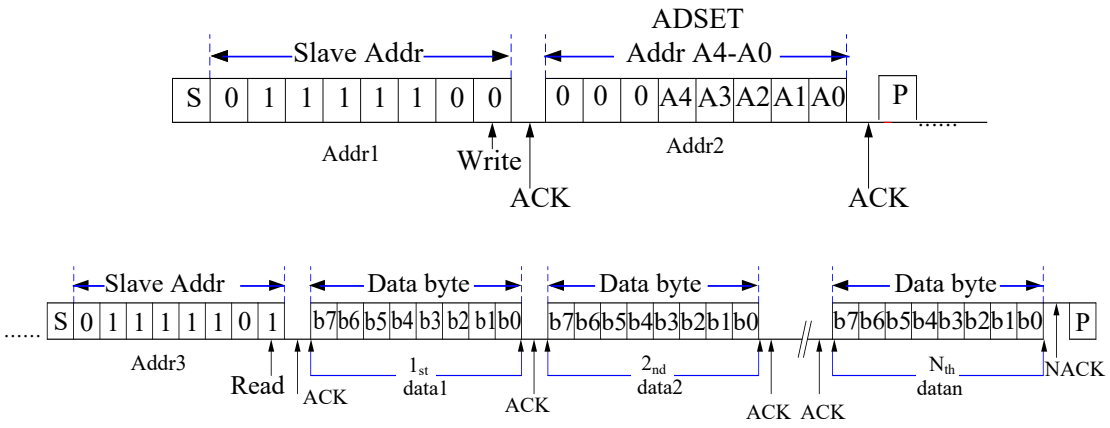
Cmd2: blinking frequency setting command - Set as needed. If the flicker does not need to be changed, this byte does not have to be sent

Addr2: Address setting command - Set the display RAM starting address (0x0B)

Data1-Datan: Send the display data to the starting address and subsequent address of the set display RAM (up to 8 bytes)

STOP: Send the I2C stop signal

8.3 Read the display data



START: Send the I2C start signal

Addr1: Send the Slave address (0x7c)

Addr2: Address setting command - Set the display RAM starting address (0x0B)

STOP: Send the I2C stop signal

START: Send the I2C start signal

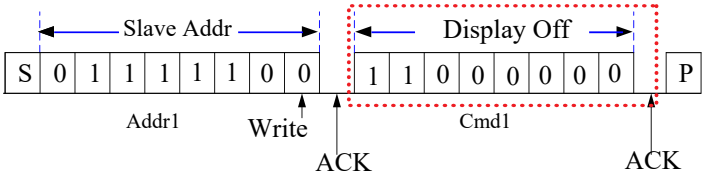
Addr3 : Send the Slave address (0x7d bit1=1 read)

Data1-Datan: Read data from display RAM

STOP: Send the I2C stop signal

8.4 Display Off

Other commands can also be sent in this format.



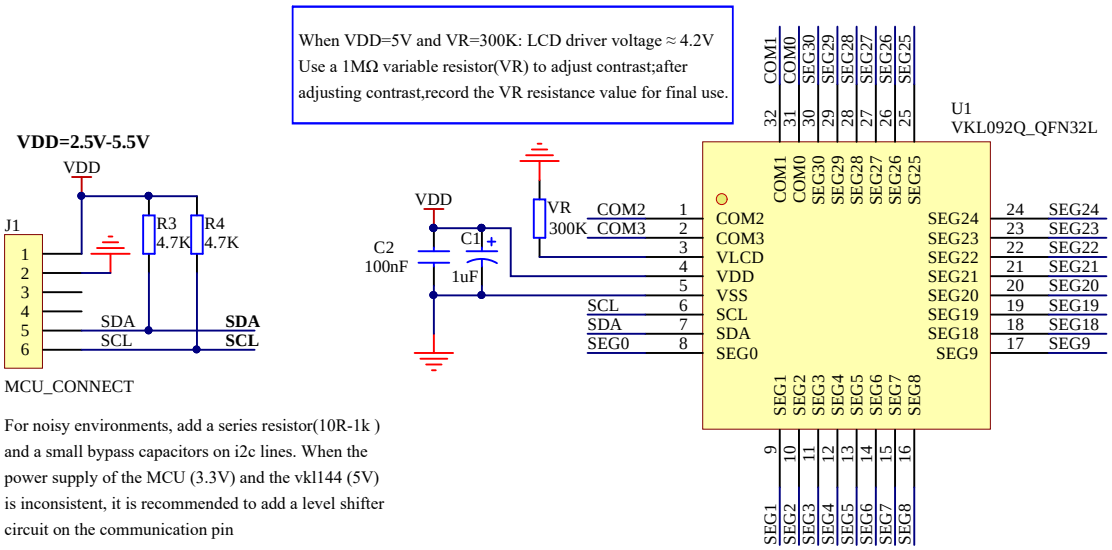
START: Send the I2C start signal

Addr1: Send the Slave address (0x7c)

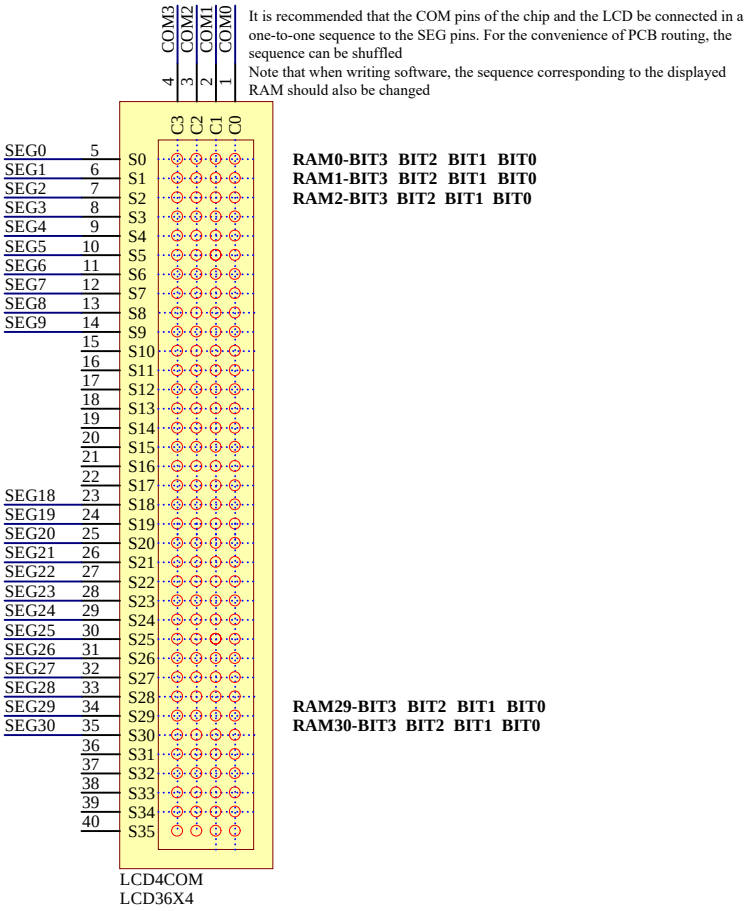
Cmd1: Mode setting command - Display Off (0xC0)

STOP: Send the I2C stop signal

9 Application Circuits



For noisy environments, add a series resistor(10R-1k) and a small bypass capacitors on i2c lines. When the power supply of the MCU (3.3V) and the vkl144 (5V) is inconsistent, it is recommended to add a level shifter circuit on the communication pin



It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequence to the SEG pins. For the convenience of PCB routing, the sequence can be shuffled
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed

RAM0-BIT3 BIT2 BIT1 BIT0
RAM1-BIT3 BIT2 BIT1 BIT0
RAM2-BIT3 BIT2 BIT1 BIT0

RAM29-BIT3 BIT2 BIT1 BIT0
RAM30-BIT3 BIT2 BIT1 BIT0

10 Electrical Characteristics

10.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～6.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

10.2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.5	—	5.5	V	—	—
Operating current	I_{DD1}	—	7.5	20	μA	3V	VDD=3.3V, 25℃, 1/3 BIAS Power-saving Mode 1(LP1) FRAME rate 80Hz, FRAME flip.
Standby Current	I_{STB}	—	0.5	5	μA	3V	LCD display off Internal RC oscillator off.
VLCD pin voltage*1	VLCD	0	—	VDD-2.4	V	2.5V-5.5V	VDD-VLCD>=2.5V
Low-level Input	V_{IL}	0	—	0.3	VDD	3V 5V	SCL, SDA
High-level Input	V_{IH}	0.8	—	1.0	VDD	3V 5V	SCL, SDA
"L" input current	I_{IL}	-1	—	—	μA	3V	—
"H" input current	I_{IH}	—	—	1	μA	3V	—
LCD ON resistor	R_{ON}	—	3	—	kΩ	3V	I_{load}=±10uA

*1 LCD voltage=VDD-VLCD

10.3 AC Electrical Characteristics

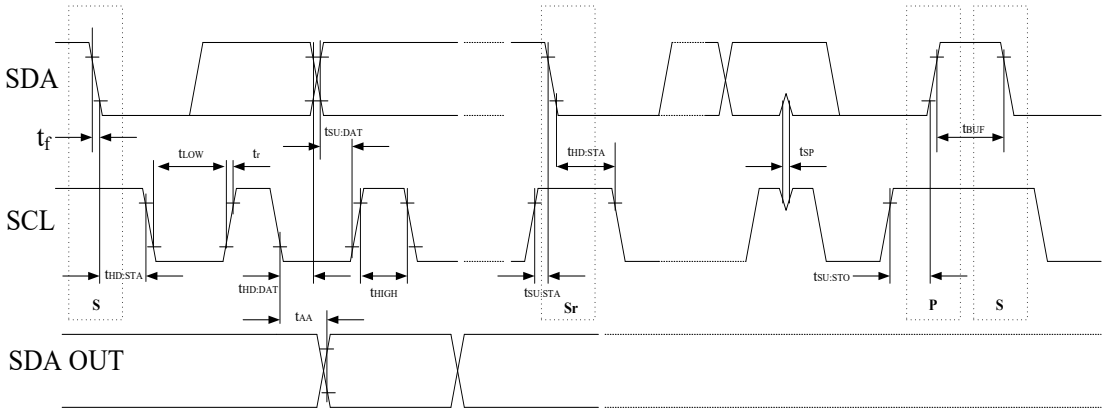
Frame Frequency

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD 帧频频率	f_{LCD1}	56	80	104	Hz	3.3V	Frame rate 80Hz,-40 ~ +85℃
LCD 帧频频率	f_{LCD2}	49	71	93	Hz	3.3V	Frame rate 71Hz,-40 ~ +85℃
LCD 帧频频率	f_{LCD3}	44	64	84	Hz	3.3V	Frame rate 64Hz,-40 ~ +85℃
LCD 帧频频率	f_{LCD4}	37	53	69	Hz	3.3V	Frame rate 53Hz,-40 ~ +85℃

I2C parameter

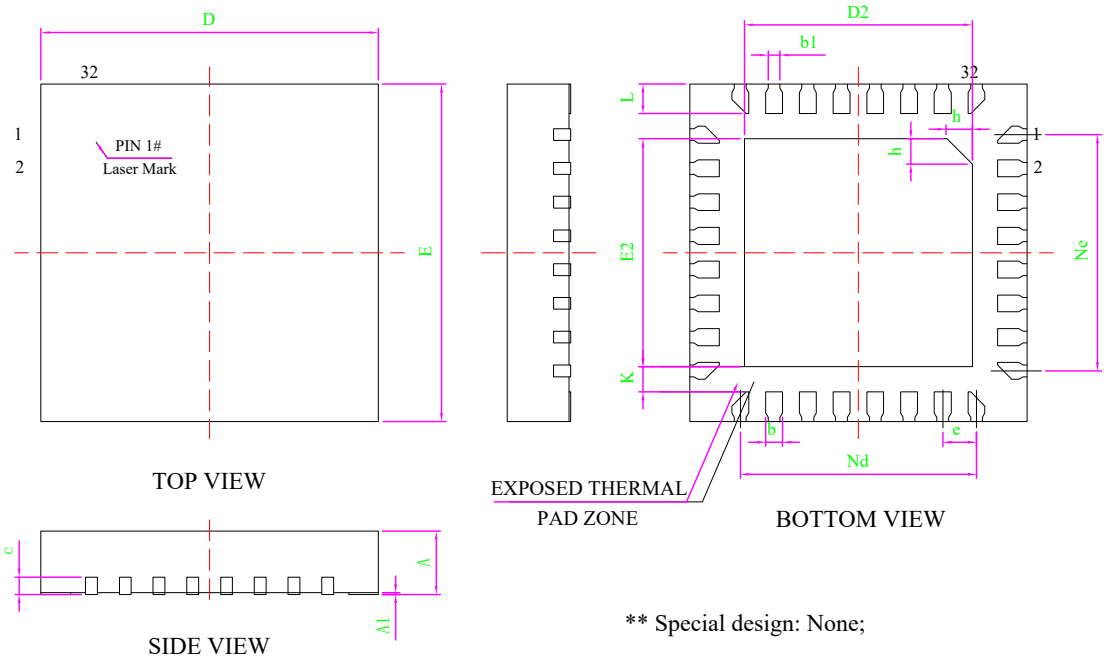
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	f_{SCL}	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	t_{BUF}	1.3	—	—	μs	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	$t_{HD:STA}$	0.6	—	—	μs	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	t_{LOW}	1.3	—	—	μs	3.0-5.5V	—
SCL High Time	t_{HIGH}	0.6	—	—	μs	3.0-5.5V	—
Start Condition Setup Time	$t_{SU:STA}$	0.6	—	—	μs	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	$t_{HD:DAT}$	0	—	—	ns	3.0-5.5V	—
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	t_R	—	—	0.3	μs	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	t_F	—	—	0.3	μs	3.0-5.5V	periodically sampled
Stop Condition Setup Time	$t_{SU:STO}$	0.6	—		μs	3.0-5.5V	—
Output Valid from Clock	t_{AA}	—	—	0.9	μs	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin)	t_{SP}	—	—	50	ns	3.0-5.5V	Noise suppression time

I²C Timing


SDA
SCL
SDA OUT
tf
tLOW
tr
tSU:DAT
tHD:STA
tSP
tBUF
tHD:STA
tHD:DAT
tHIGH
tAA
tSU:STA
tSU:STO
S
Sr
P
S

11 Package Information

11.1 QFN32L (4.0mm × 4.0mm PP=0.4mm)



** Special design: None;

Dimensions			
SYMBOL	MIN	NOMINAL	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
B1	0.14REF		
c	0.203REF		
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.60	2.7	2.80
Ne	2.80BSC		
L	0.30	0.35	0.40
h	0.25	0.30	0.35
K	0.30REF		

12 Disclaimer

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13 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-08-09	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/