永嘉微电
Vinka Microelectronics

VK2C24B Datasheet

55×4/51×8/43×16
LCD DRIVER
Rev.1.4

1 General Description

The VK2C24B is a dot-matrix memory-mapped LCD driver that supports LCD screens with a maximum of 220 dots (55SEG×4COM)/408 dots (51SEG×8COM)/688 dots (43SEG×16COM). The single-chip microcomputer can be configured with display parameters and read and write display data through the I2C interface, and can also enter power-saving mode through instructions. Its high anti-interference and low power consumption features make it suitable for water, electricity and gas meters as well as various industrial control instruments.

2 Key Features

- Operating voltage:2.4-5.5V
- Built-in RC oscillator (default)
- Selectable LCD bias: 1/2、1/3、1/4、1/5
- Selectable LCD duty:1/4、1/8、1/16
- Built-in 72×4-bit、68×8-bit、60×16-bitdisplay RAM
- The frame rate can be configured as 80Hz or 160Hz
- Power-down mode via software command(LCD OFF, SYS DIS)
- I2C communication interface
- Display mode 55×4/51×8/43×16
- Three display overall flicker frequencies
- Software-configurable of LCD parameters
- Auto-increment addressing for sequential read/write
- VLCD pin provides the LCD driving voltage source(2.4-5.5V)
- It is equipped with a built-in 16-stage LCD driver voltage adjustment circuit
- Built-in power-on reset circuit (POR)
- Low power consumption and high anti-interference
- Available Packages:
  LQFP64(7.0mm × 7.0mm PP=0.4mm)
  DICE
  COG

3 Product Selection

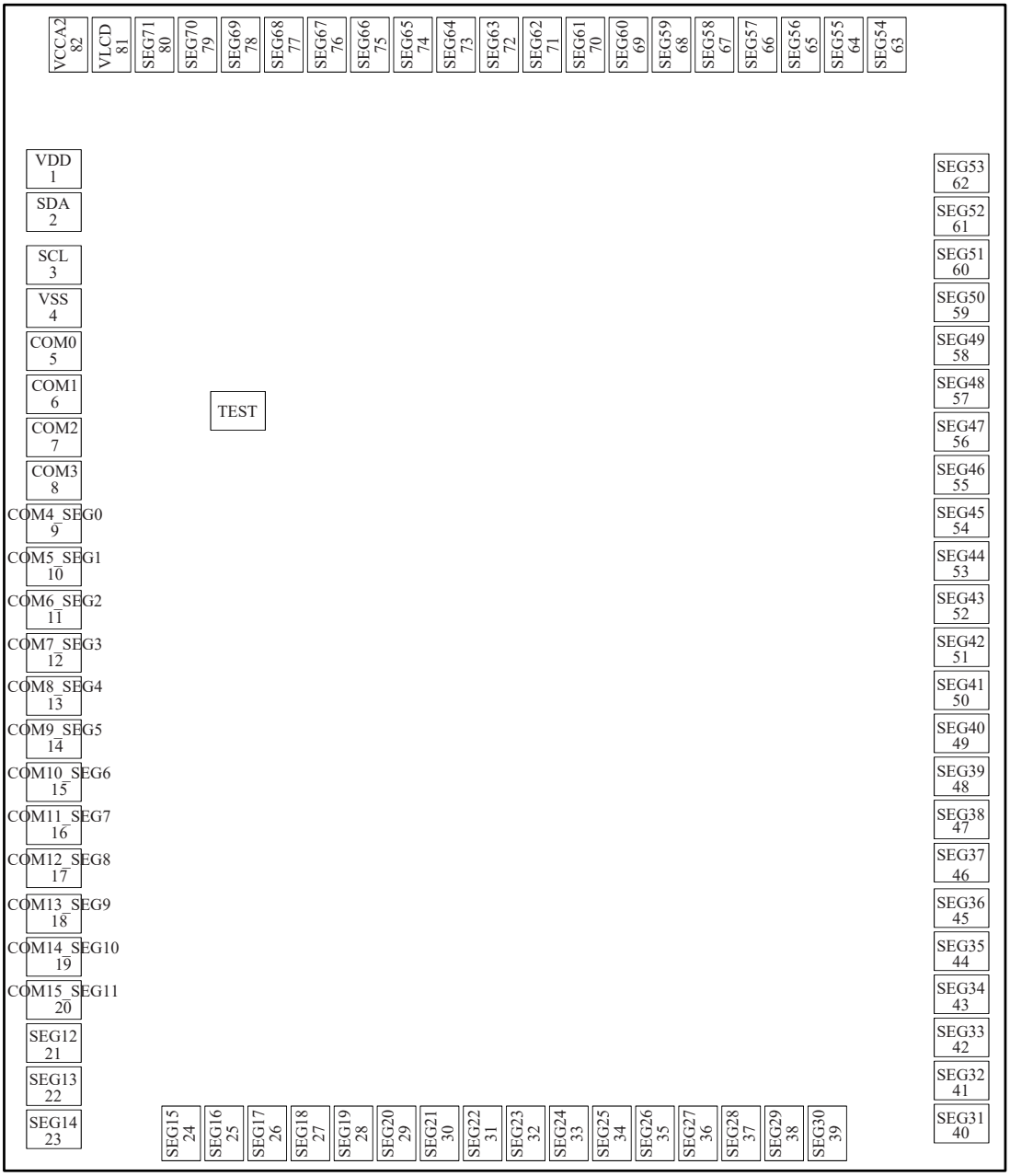
Part No.	SEG×COM	BIAS	DUTY	Packaging
VK2C21A	20×4,16×8	1/3,1/4	1/4,1/8	SOP28
VK2C21AA	20×4,16×8	1/3,1/4	1/4,1/8	SSOP28
VK2C21AQ	20×4,16×8	1/3,1/4	1/4,1/8	QFN28L
VK2C21B	16×4,12×8	1/3,1/4	1/4,1/8	SOP24
VK2C21BA	16×4,12×8	1/3,1/4	1/4,1/8	SSOP24
VK2C21BQ	16×4,12×8	1/3,1/4	1/4,1/8	QFN24L
VK2C21C	12×4,8×8	1/3,1/4	1/4,1/8	SOP20
VK2C21CQ	12×4,8×8	1/3,1/4	1/4,1/8	QFN20L
VK2C21D	8×4,4×8	1/3,1/4	1/4,1/8	SOP16
VK2C21DQ	8×4,4×8	1/3,1/4	1/4,1/8	QFN16L
VK2C22A	44×4	1/2,1/3	1/4	LQFP52
VK2C22B	40×4	1/2,1/3	1/4	LQFP48
VK2C22	44×4	1/2,1/3	1/4	DICE
VK2C23A	55×4,51×8	1/3,1/4	1/4, 1/8	LQFP64
VK2C23B	35×8	1/3,1/4	1/8	LQFP48
VK2C23	56×4,52×8	1/3,1/4	1/4,1/8	DICE
VK2C24A	71×4,67×8,59×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	LQFP80
VK2C24B	55×4,51×8,43×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	LQFP64
VK2C24	72×4,68×8,60×16	1/2,1/3,1/4,1/5	1/4,1/8,1/16	DICE

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray(reel)Qty	Box Qty	Total Qty	Notes
VK2C21A	SOP28	26/tube	-	2080/box	20800 PCS	
VK2C21AA	SSOP28	50/tube	-	5000/box	50000 PCS	
VK2C21AQ	QFN28L	-	490/reel	4900/box	29400 PCS	
VK2C21B	SOP24	30/tube	-	2400/box	24000 PCS	
VK2C21BA	SSOP24	50/tube	-	10000/box	100000 PCS	
VK2C21BQ	QFN24L	-	490/reel	4900/box	29400 PCS	
VK2C21C	SOP20	36/tube	-	2880/box	28800 PCS	
VK2C21CQ	QFN20L	-	490/reel	4900/box	29400 PCS	
VK2C21D	SOP16	50/tube	-	10000/box	100000 PCS	
VK2C21DQ	QFN16L	-	3000/reel	3000/box	120000 PCS	
VK2C22A	LQFP52	-	90/tray	900/box	5400 PCS	
VK2C22B	LQFP48	-	250/tray	2500/box	15000 PCS	
VK2C22	DICE	-	400/tray	2000/box	4000 PCS	DICE
VK2C23A	LQFP64	-	250/tray	2500/box	15000 PCS	
VK2C23B	LQFP48	-	250/tray	2500/box	15000 PCS	
VK2C23	DICE	-	250/tray	1000/box	2000 PCS	DICE
VK2C24A	LQFP80	-	90/tray	900/box	5400 PCS	
VK2C24B	LQFP64	-	250/tray	2500/box	15000 PCS	
VK2C24	DICE	-	200/tray	1000/box	2000 PCS	DICE

5 COB Pad Information

5.1 COB Pad Assignment



Original:(0，0)；Chip Size X=2000um； Y=2300um；

This area does not include the cutting track. The size of the slicing track is 60um*60um，

Die Size X=2060um； Y=2360um； Substrate potential: GND

When VLCD pad and VCCA2 pad are bound together, VLCD≤+5.5V(VLCD can be connected to an external voltage source to achieve VLCD≥VDD)

Built-in voltage setting (IVA) command		VLCD	SEG71	Note
DE	VE			
0	0	Input	Null	• VLCD supports internal bias voltage
0	1	Input	Null	• The internal voltage is adjusted to Null • VLCD supports internal bias voltage
1	0	Input	Output	• VLCD supports internal bias voltage
1	1	Input	Output	• VLCD supports internal bias voltage

When VDD pad and VCCA2 pad are bound together, VLCD≤VDD

Built-in voltage setting (IVA) command		VLCD	SEG71	Note
DE	VE			
0	0	Input	Null	• VLCD supports internal bias voltage
0	1	Output	Null	• Detect the internal bias voltage *1 • VDD supports internal bias voltage
1	0	NC	Output	• VDD supports internal bias voltage
1	1	NC	Output	• VDD supports internal bias voltage

5.2 COB PAD Coordinates

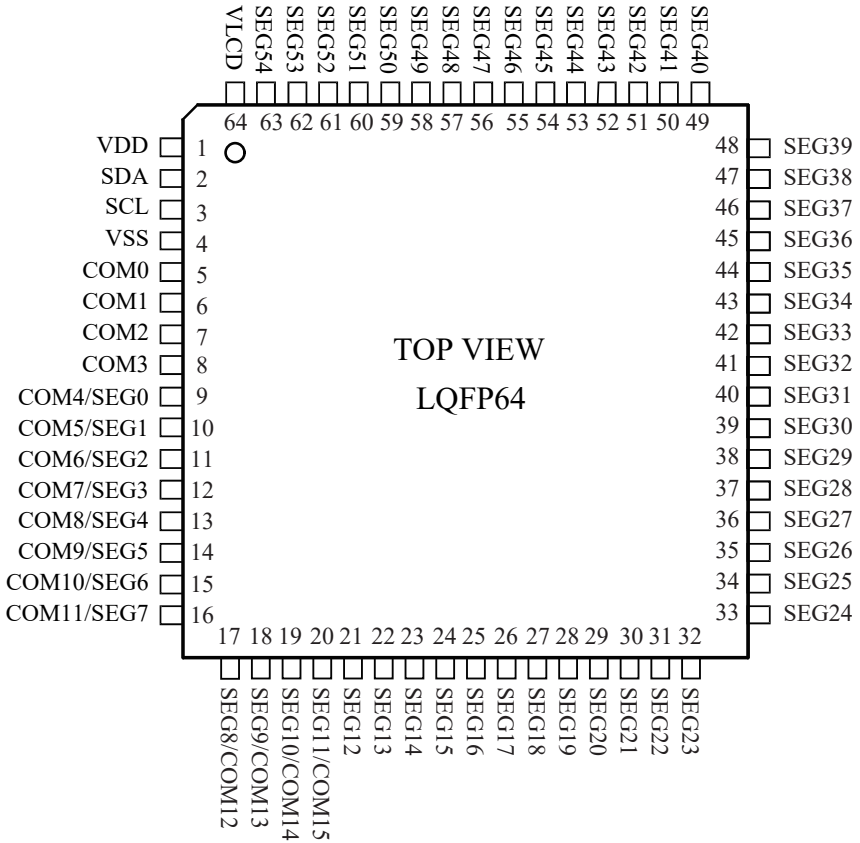
Unit: um

No.	PAD NAME	PAD SIZE (um^2)	X (Center)um	Y (Center)um	NOTE
1	VDD	70*70	93.36	1990.42	
2	SDA	70*70	93.36	1905.92	
3	SCL	70*70	93.36	1807.42	
4	VSS	70*70	93.36	1722.92	
5	COM0	70*70	93.36	1638.42	
6	COM1	70*70	93.36	1543.92	
7	COM2	70*70	93.36	1459.42	
8	COM3	70*70	93.36	1374.92	
9	COM4_SEG0	70*70	93.36	1290.42	
10	COM5_SEG1	70*70	93.36	1205.92	
11	COM6_SEG2	70*70	93.36	1121.42	
12	COM7_SEG3	70*70	93.36	1036.92	
13	COM8_SEG4	70*70	93.36	952.42	

14	COM9_SEG5	70*70	93.36	867.92	
15	COM10_SEG6	70*70	93.36	783.42	
16	COM11_SEG7	70*70	93.36	698.92	
17	COM12_SEG8	70*70	93.36	614.42	
18	COM13_SEG9	70*70	93.36	529.92	
19	COM14_SEG10	70*70	93.36	445.42	
20	COM15_SEG11	70*70	93.36	360.92	
21	SEG12	70*70	93.36	276.42	
22	SEG13	70*70	93.36	191.92	
23	SEG14	70*70	93.36	107.42	
24	SEG15	70*70	368.04	93.36	
25	SEG16	70*70	452.54	93.36	
26	SEG17	70*70	537.04	93.36	
27	SEG18	70*70	621.54	93.36	
28	SEG19	70*70	706.04	93.36	
29	SEG20	70*70	790.54	93.36	
30	SEG21	70*70	875.04	93.36	
31	SEG22	70*70	959.54	93.36	
32	SEG23	70*70	1044.04	93.36	
33	SEG24	70*70	1128.54	93.36	
34	SEG25	70*70	1213.04	93.36	
35	SEG26	70*70	1297.54	93.36	
36	SEG27	70*70	1382.04	93.36	
37	SEG28	70*70	1466.54	93.36	
38	SEG29	70*70	1551.04	93.36	
39	SEG30	70*70	1635.54	93.36	
40	SEG31	70*70	1906.64	107.42	
41	SEG32	70*70	1906.64	191.92	
42	SEG33	70*70	1906.64	276.42	
43	SEG34	70*70	1906.64	360.92	
44	SEG35	70*70	1906.64	445.42	
45	SEG36	70*70	1906.64	529.92	
46	SEG37	70*70	1906.64	614.42	
47	SEG38	70*70	1906.64	698.92	
48	SEG39	70*70	1906.64	783.42	

49	SEG40	70*70	1906.64	867.92	
50	SEG41	70*70	1906.64	952.42	
51	SEG42	70*70	1906.64	1036.92	
52	SEG43	70*70	1906.64	1121.42	
53	SEG44	70*70	1906.64	1205.92	
54	SEG45	70*70	1906.64	1290.42	
55	SEG46	70*70	1906.64	1374.92	
56	SEG47	70*70	1906.64	1459.42	
57	SEG48	70*70	1906.64	1543.92	
58	SEG49	70*70	1906.64	1628.42	
59	SEG50	70*70	1906.64	1712.92	
60	SEG51	70*70	1906.64	1797.42	
61	SEG52	70*70	1906.64	1881.92	
62	SEG53	70*70	1906.64	1966.42	
63	SEG54	70*70	1757.54	2206.64	
64	SEG55	70*70	1673.04	2206.64	
65	SEG56	70*70	1588.54	2206.64	
66	SEG57	70*70	1504.04	2206.64	
67	SEG58	70*70	1419.54	2206.64	
68	SEG59	70*70	1335.04	2206.64	
69	SEG60	70*70	1250.54	2206.64	
70	SEG61	70*70	1166.04	2206.64	
71	SEG62	70*70	1081.54	2206.64	
72	SEG63	70*70	997.04	2206.64	
73	SEG64	70*70	912.54	2206.64	
74	SEG65	70*70	828.04	2206.64	
75	SEG66	70*70	743.54	2206.64	
76	SEG67	70*70	659.04	2206.64	
77	SEG68	70*70	574.54	2206.64	
78	SEG69	70*70	490.04	2206.64	
79	SEG70	70*70	393.04	2206.64	
80	SEG71	70*70	303.04	2206.64	
81	VLCD	70*70	210.43	2206.64	
82	VCCA2	70*70	125.93	2206.64	
83	TEST	70*70	464.01	1521.21	test pad

6 Package Pinout Information(LQFP64)



Note: The VCCA2 pad is internally connected to the VLCD pad;
the OP pad is left floating(NC)

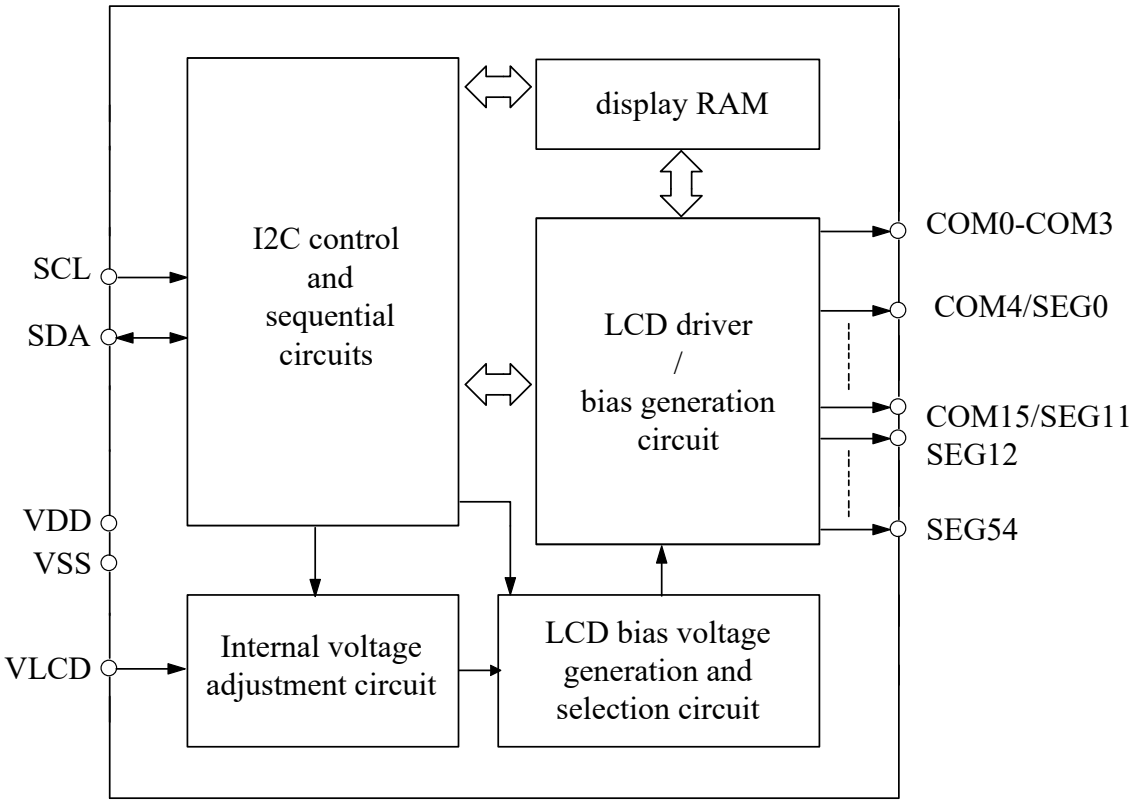
For more information: Page 26

6.1 VK2C24B/LQFP64 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	Positive power supply
2	SDA	I/O	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	Negative power supply
5-8	COM0-COM3	O	LCD COM drive outputs
9-20	COM4/SEG0- COM15/SEG11	O	LCD COM/SEG drive outputs, software configuration: 4COM or 8/16COM
21-63	SEG12-SEG54	O	LCD SEG drive outputs
64	VLCD	I	When the VLCD pin and VDD pin are short-circuited and the internal voltage regulation function is enabled, the drive voltage is regulated by the internal voltage regulation function. When the VLCD pin is connected in series with the VDD pin and the internal voltage adjustment function is disabled, the LCD driving voltage is set by the series resistor.

7 Functional Description

7.1 Block Diagram



7.2 Display RAM

The display RAM is organized as 60×16 bits (or 76×4 bits for 4-COM mode and 68×8 bits for 8-COM mode), storingthe displayed data. The content of the display RAM is directly mapped to the display content of the LCD driver. Display RAM data is accessed via I2C commands.

The following is a mapping from the RAM to the LCD pattern:

Output	COM15	COM14	COM13	COM12	COM11	COM10	COM9	COM8	Addr	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	Addr
SEG12									01H									00H
SEG13									03H									02H
SEG14									05H									04H
SEG15									07H									06H
SEG16									09H									08H
SEG17									0BH									0AH
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG71									77H									76H
	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0	Data

RAM Mapping of 60×16

Output	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	Address
SEG4									00H
SEG5									01H
SEG6									02H
SEG7									03H
SEG8									04H
SEG9									05H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG71									43H
	D7	D6	D5	D4	D3	D2	D1	D0	Data

RAM Mapping of 68×8

Output	COM3	COM2	COM1	COM0	Output	COM3	COM2	COM1	COM0	Address
SEG1					SEG0					00H
SEG3					SEG2					01H
SEG5					SEG4					02H
SEG7					SEG6					03H
SEG9					SEG8					04H
SEG11					SEG11					05H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG71					SEG70					25H
	D7	D6	D5	D4		D3	D2	D1	D0	Data

RAM Mapping of 76×4

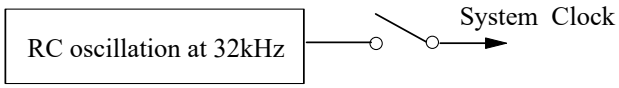
7.3 System Oscillator

The clock of VK2C24B is used to generate LCD drive signals and internal logic timing. The system clock is derived from the internal RC oscillator (32kHz), and the system clock frequency (f_{SYS}) determines the LCD frame frequency.

The system setting command can start or stop the system oscillator. After the display shows off and the system oscillator stops, the system enters the power-saving mode.

When the system is powered on and working, the system oscillator is in a stopped state.

The Settings of the system oscillation are shown in the following figure:



7.4 LCD operating voltage

The LCD driver voltage can be obtained through the VLCD pin or selected as a 16-level voltage through the internal configuration.

When the VLCD pad is connected to the VCCA2 pad, the LCD driving voltage can be supplied from an external voltage source (VLCD≤5.5V),and VLCD may be higher than VDD.

When the VDD pad is connected to the VCCA2 pad, the LCD driving voltage can be obtained by connecting the VLCD pin to VDD through a series resistor (VLCD≤VDD).

The internal 16-level voltage is set through a 4-bit programmable analog switch, as shown in the following table:When VCCA2 pad is connected to VDD pad

Bias / DA3~DA0	1/1	1/2	1/3	1/4	1/5	Note
00H	1.000	1.000	1.000	1.000	1.000	Default
01H	0.849	0.918	0.944	0.957	0.966	
02H	0.738	0.849	0.894	0.918	0.934	
03H	0.652	0.789	0.849	0.882	0.904	
04H	0.584	0.738	0.808	0.849	0.875	
05H	0.529	0.692	0.771	0.818	0.849	
06H	0.484	0.652	0.738	0.789	0.824	
07H	0.446	0.616	0.707	0.763	0.801	
08H	0.413	0.584	0.678	0.738	0.779	
09H	0.385	0.556	0.652	0.714	0.758	
0AH	0.360	0.529	0.628	0.692	0.738	
0BH	0.338	0.506	0.605	0.672	0.719	
0CH	0.319	0.484	0.584	0.652	0.701	
0DH	0.302	0.464	0.565	0.634	0.684	
0EH	0.287	0.446	0.547	0.616	0.668	
0FH	0.273	0.429	0.529	0.600	0.652	

When the VCCA2 pad is connected to the VLCD pad

Bias / DA3~DA0	1/1	1/2	1/3	1/4	1/5
0x00(Default)	1.000×VLCD	1.000×VLCD	1.000×VLCD	1.000×VLCD	1.000×VLCD
0x01	0.849×VLCD	0.918×VLCD	0.944×VLCD	0.957×VLCD	0.966×VLCD
0x02	0.738×VLCD	0.849×VLCD	0.894×VLCD	0.918×VLCD	0.934×VLCD
0x03	0.652×VLCD	0.789×VLCD	0.849×VLCD	0.882×VLCD	0.904×VLCD
0x04	0.584×VLCD	0.738×VLCD	0.808×VLCD	0.849×VLCD	0.875×VLCD
0x05	0.529×VLCD	0.692×VLCD	0.771×VLCD	0.818×VLCD	0.849×VLCD
0x06	0.484×VLCD	0.652×VLCD	0.738×VLCD	0.789×VLCD	0.824×VLCD
0x07	0.446×VLCD	0.616×VLCD	0.707×VLCD	0.763×VLCD	0.801×VLCD
0x08	0.413×VLCD	0.584×VLCD	0.678×VLCD	0.738×VLCD	0.779×VLCD
0x09	0.385×VLCD	0.556×VLCD	0.652×VLCD	0.714×VLCD	0.758×VLCD
0x0A	0.360×VLCD	0.529×VLCD	0.628×VLCD	0.692×VLCD	0.738×VLCD
0x0B	0.338×VLCD	0.506×VLCD	0.605×VLCD	0.672×VLCD	0.719×VLCD
0x0C	0.319×VLCD	0.484×VLCD	0.584×VLCD	0.652×VLCD	0.701×VLCD
0x0D	0.302×VLCD	0.464×VLCD	0.565×VLCD	0.634×VLCD	0.684×VLCD
0x0E	0.287×VLCD	0.446×VLCD	0.547×VLCD	0.616×VLCD	0.668×VLCD
0x0F	0.273×VLCD	0.429×VLCD	0.529×VLCD	0.600×VLCD	0.652×VLCD

7.5 Power-On Reset

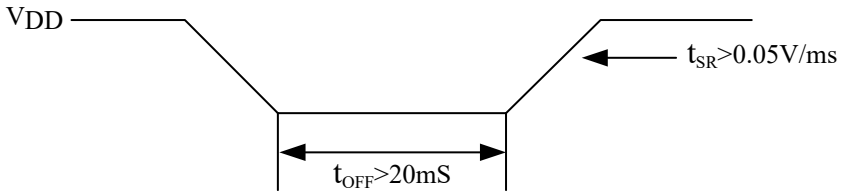
During the initialization of the power-on reset circuit(1ms),no I2C data transmission should occur.

The state of the internal circuit after initialization is as follows:

- When VLCD≤VDD, all COM/SEG pins output VDD.
- When VDD≤VLCD, all COM/SEG pins output VLCD.
- Configure 1/4 duty and 1/3 bias.
- The system oscillator and LCD bias generator are turned off.
- The LCD display is off.
- The internal voltage adjustment function is enabled.
- Set the shared pin of SEG/VLCD as the SEG pin.
- The VLCD pin detection function is prohibited.
- The frame rate is configured to 80Hz by default.
- Flashing function prohibited.

If,during operation, VDD falls below the specified minimum operating voltage, the power-on reset timing requirements must be met, that is, the VDD voltage must drop to 0V and remain at 0V for at least 20ms before rising to the normal operating voltage

Power-on Reset Timing：



7.6 LCD Communication Command

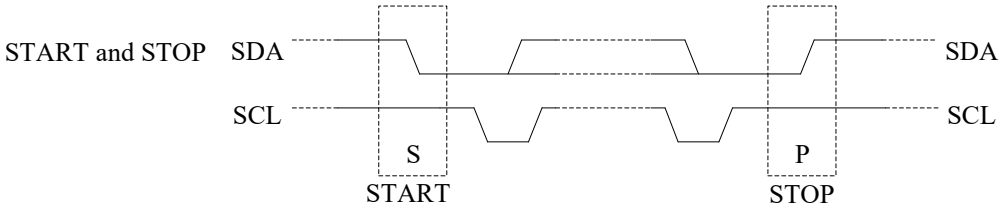
The LCD driver supports 71SEG×4COM、67SEG×8COM、 59SEG×16COM modes, any unused SEG and COM pins should be left floating(NC).

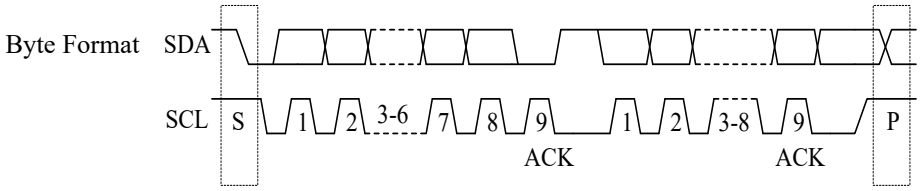
Two frame frequencies are provided, and you can choose to set them to 80Hz or 160Hz through the frame frequency setting command.

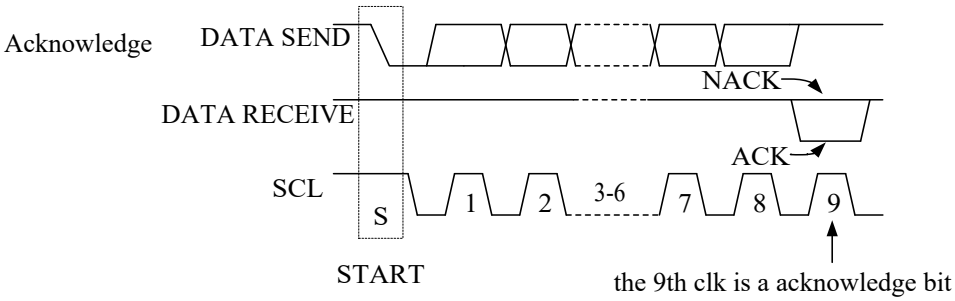
8 I2C Serial Interface

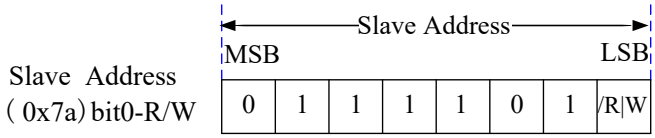
The VK2C24B features two communication pins compliant with the I2C protocol. open-drain outputs require external pull-up resistors.

The SCL pin is the clock input pin, and the SDA pin is the serial data input/output pin. When the I2C bus is idle, both pins remain at a logic high level.





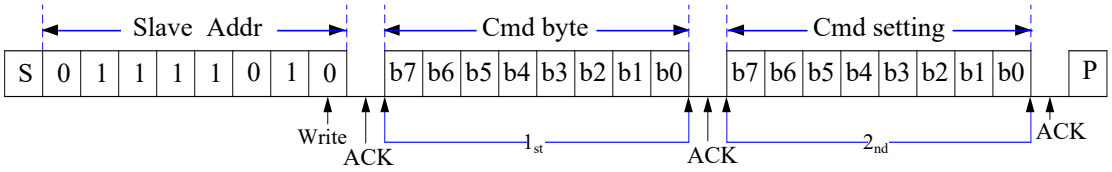




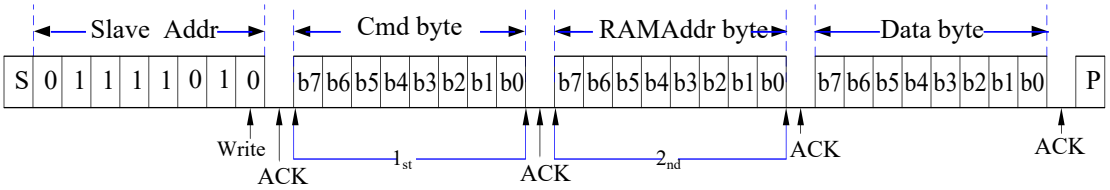
9 I2C Command Format

Write operation

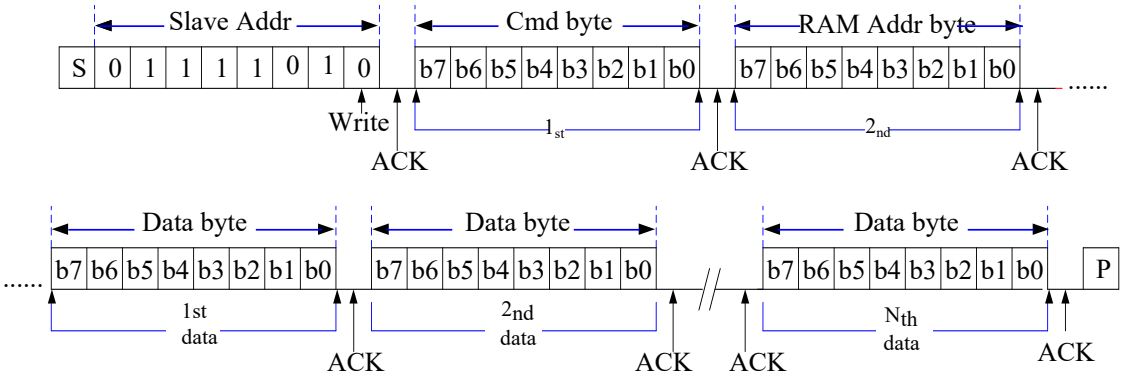
Write commands



Write a single byte to the display RAM

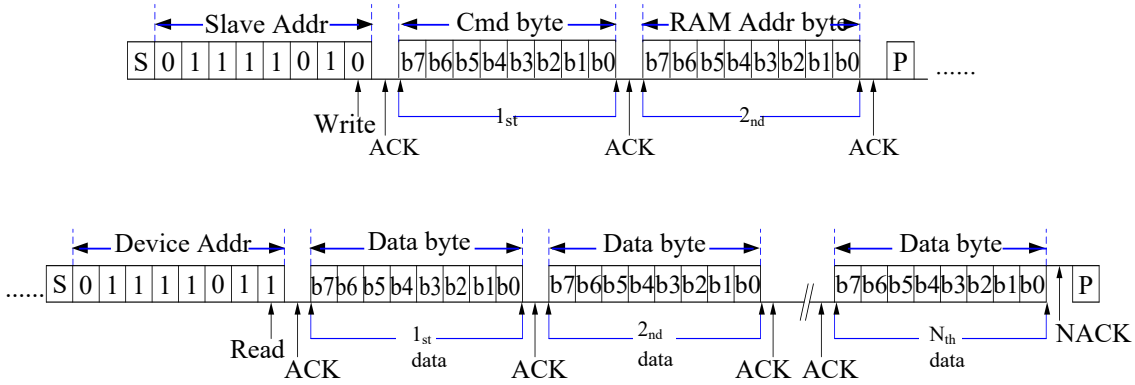


Write multiple bytes to the display RAM

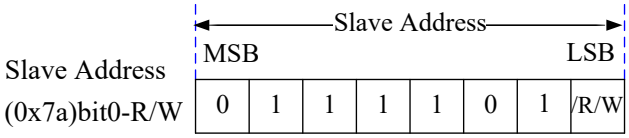


Read operation

Read multiple bytes from the display RAM



10 Command Summary



10.1 Display Data Command

Send display data to display RAM

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Display data command	1st	1	0	0	0	0	0	0	0		W	
Address pointer	2nd	X	A6	A5	A4	A3	A2	A1	A0	Display data start address	W	00H

10.2 Mode Set Command

Set BIAS and DUTY

Function	Byte	(MSB)Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	(LSB)Bit0
Driver mode setting command	1st	1	0	0	0	0	0	1	0
Duty and Bias	2nd	X	X	Duty2	X	Duty1	Bias1	Duty0	Bias0

Bit 5	Bit 3	Bit 1	Duty
Duty2	Duty1	Duty0	
0	0	0	1/4 duty
0	0	1	1/8 duty
0	1	0	1/16 duty

Bit 2	Bit0	Bias
Bias1	Bias0	
0	0	1/3 bias
0	1	1/4 bias
1	0	1/5 bias
1	1	1/2 bias

10.3 System Settings Command

Enable/disable the internal system oscillator and LCD display

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
System Settings Command	1st	1	0	0	0	0	1	0	0		W	
System oscillator and Display the on/off Settings	2nd	X	X	X	X	X	X	S	E		W	00H

Bit 1	Bit 0	Internal system oscillator	LCD display
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

10.4 Frame rate setting command

Select the frame frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Frame frequency command	1st	1	0	0	0	0	1	1	0		W	
Frame frequency setting	2nd	X	X	X	X	X	X	X	F		W	00H

Bit 0	Frame frequency
F	
0	80Hz
1	160Hz

10.5 Blinking Frequency Command

Set the blinking frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Blinking frequency command	1st	1	0	0	0	1	0	0	0		W	
Blinking frequency setting	2nd	X	X	X	X	X	X	BK1	BK0		W	00H

Bit 1	Bit 0	blinking freq
BK1	BK0	
0	0	blinking off(Def)
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

10.6 Internal Voltage Adjustment(IVA) Command

The IVA command allows selection of 16 voltage levels to adjust the LCD driver voltage

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
IVA Com	1st	1	0	0	0	1	0	1	0		W	
IVA set	2nd	X	X	DE	VE	DA3	DA2	DA1	DA0	The SEG/VLCD pin function is set through the DE bit. The VE bit enables or disables the internal voltage adjustment function. DA3 to DA0 are used to adjust the output voltage of the VLCD.	W	30H

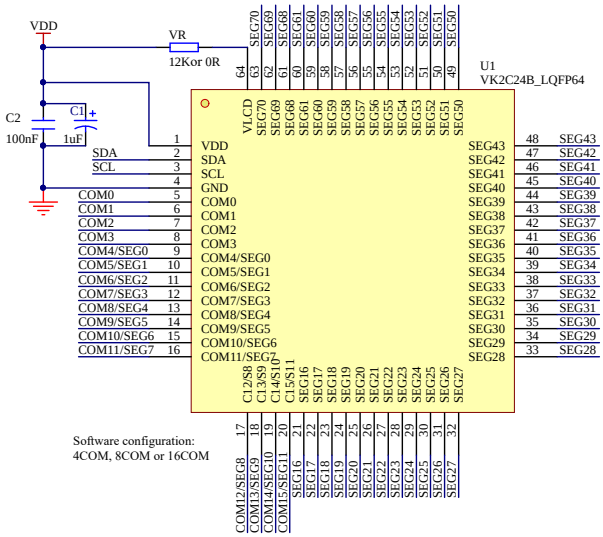
Note：

Bit 5	Bit 4	SEG71/VLCD shared pin sel	internal voltage adjustment	Note
DE	VE			
0	0	VLCD pin	off	• VCCA2→VLCD: bias voltage is provided by VLCD pin • VCCA2→VDD: bias voltage is provided by VLCD pin. • Note:VLCD→VDD: disable the internal voltage follower by setting DA3- DA0 to "0000".
0	1	VLCD pin	on	• VCCA2→VLCD: Internal voltage adjustment disabled. (bias voltage is provided by VLCD pin) • VCCA2→VDD:bias voltage is provided by VLCD • pin,Internal adjustment disabled. (Not recommended.) • VCCA2→VDD:VLCD floating,Internal adjustment enabled. (internal regulation adjusts bias)
1	0	SEG71 pin/COB	off	• VCCA2→VLCD: bias voltage is provided by VLCD pin • VCCA2→VDD: bias voltage is provided by VDD pin. Note:Internal voltage follower is automatically disabled, ignore DA3 to DA0 bits.
1	1	SEG71 pin/COB	on	• VCCA2→VLCD: bias voltage is provided by VLCD,internal regulation adjusts bias. • VCCA2→VDD:bias voltage is provided by VDD,internal regulation adjusts bias.

- Power-on status: The internal voltage adjustment function is enabled and the SEG/VLCD pin is selected as the SEG pin.
- When the DA0 to DA3 bits are set to "0000", the internal voltage follower is prohibited.
- When the DA0 to DA3 bits are set to values other than "0000", the internal voltage follower is enabled.

11 Application Circuits

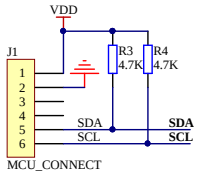
1. The software configuration bias voltage is achieved through the internal voltage adjustment function: VLCD and VDD are short-circuited, VR = 0R.
2. When the software configuration bias voltage is provided by the VLCD pin: (VLCD can be connected to a power supply less than 5.5V through VR, and VLCD can be greater than VDD)
When VLCD is connected to VDD through VR and VDD = 5V, VR = 12K: VLCD is approximately 4.2V
It is recommended to use a 20K adjustable resistor to adjust VR to achieve the best display effect, and take the resistance value at this time.



Software configuration:
4COM, 8COM or 16COM

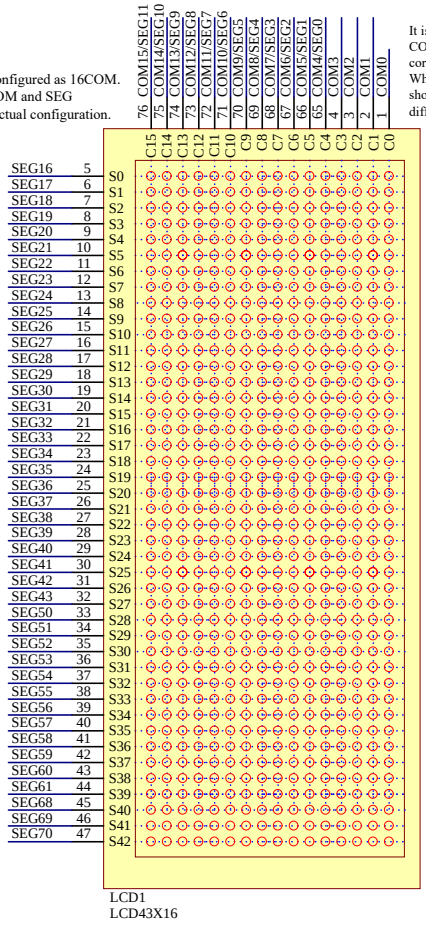
When there is a lot of external interference, a 10R to 1k resistor and a pF-level ground capacitor can be connected in series to the communication pin. When the power supply voltages of the single-chip microcontroller (3.3V) and the driver chip (5V) are inconsistent, it is recommended to add a level conversion circuit to the communication pin.

VDD=2.4V-5.5V



The software is configured as 16COM. Please connect COM and SEG according to the actual configuration.

It is recommended that the COM pins of the chip and the COM pins of the LCD be connected in a 1-to-1 correspondence.
When writing the software, the order of displaying RAM should also be changed. The SEG pins can be arranged in a different order for the convenience of PCB wiring.

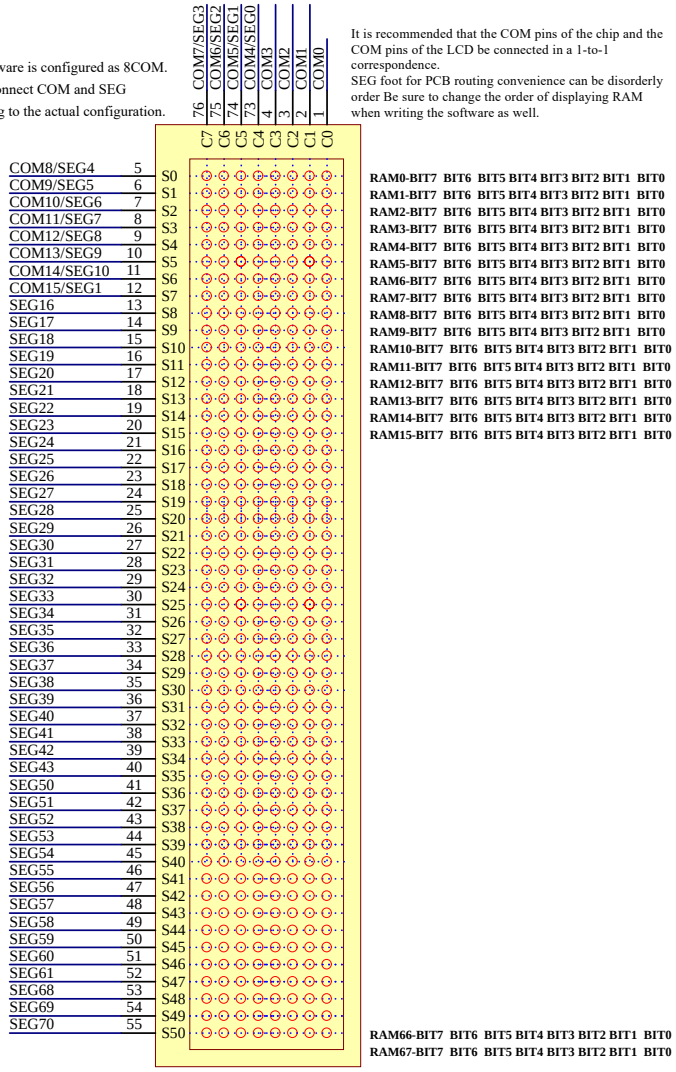


RAM0-BIT7->BIT0 **RAM1-BIT7->BIT0**
RAM2-BIT7->BIT0 **RAM3-BIT7->BIT0**
RAM4-BIT7->BIT0 **RAM5-BIT7->BIT0**
RAM6-BIT7->BIT0 **RAM7-BIT7->BIT0**
RAM8-BIT7->BIT0 **RAM9-BIT7->BIT0**
RAM10-BIT7->BIT0 **RAM11-BIT7->BIT0**
RAM12-BIT7->BIT0 **RAM13-BIT7->BIT0**
RAM14-BIT7->BIT0 **RAM15-BIT7->BIT0**

RAM116-BIT7->BIT0 **RAM117-BIT7->BIT0**
RAM118-BIT7->BIT0 **RAM119BIT7->BIT0**

The software is configured as 8COM.
Please connect COM and SEG
according to the actual configuration.

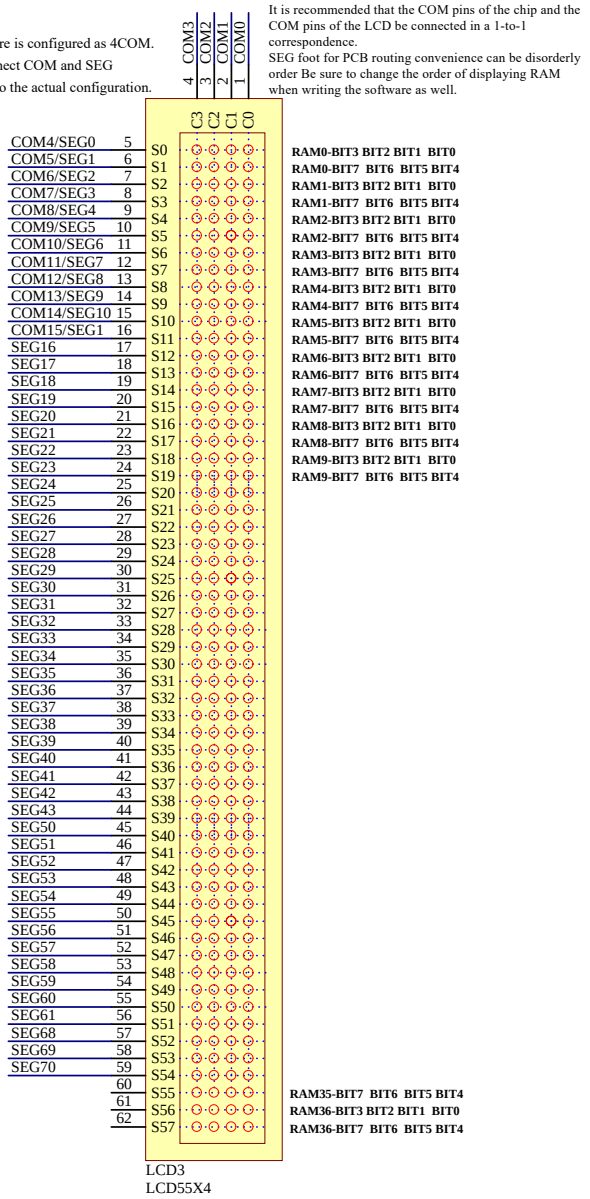
It is recommended that the COM pins of the chip and the COM pins of the LCD be connected in a 1-to-1 correspondence.
SEG foot for PCB routing convenience can be disorderly order Be sure to change the order of displaying RAM when writing the software as well.



LCD2
LCD51X8

The software is configured as 4COM.
Please connect COM and SEG
according to the actual configuration.

It is recommended that the COM pins of the chip and the COM pins of the LCD be connected in a 1-to-1 correspondence.
SEG foot for PCB routing convenience can be disorderly order Be sure to change the order of displaying RAM when writing the software as well.



LCD3
LCD55X4

12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～6.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

12.2 DC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.5	V	—	—
Operating current	I_{DD1}	—	25	40	μA	3V	No load,VLCD=VDD,1/3 bias, fLCD=80Hz,LCD off,Internal osc on,DA0~DA3 = "0000"
		—	35	50		5V	
Operating current	I_{DD2}	—	2	5	μA	3V	No load,VLCD=VDD,1/3 bias, fLCD=80Hz,LCD off,Internal osc on,DA0~DA3 = "0000"
		—	4	10		5V	
Standby Current	I_{STB}	—	—	1	μA	3V	No load, VLCD=VDD, LCD off, Internal osc off
		—	—	2		5V	
Low-level Input	V_{IL}	0	—	0.3	VDD	3V	SCL, SDA
						5V	
High-level Input	V_{IH}	0.7	—	1.0	VDD	3V	SCL, SDA
						5V	
Low Level Output Current	I_{OL}	3.0	—	—	mA	3V	V_{OL}=0.4V，SDA
		6.0	—	—		5V	
LCD COM Sink Current	I_{OL1}	250	400	—	μA	3V	V_{OL}=0.3V
		500	800	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH1}	-140	-230	—	μA	3V	V_{OH}=2.7V
		-300	-500	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL2}	250	400	—	μA	3V	V_{OL}=0.3V
		500	800	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH2}	-140	-230	—	μA	3V	V_{OH}=2.7V
		-300	-500	—		5V	V_{OH}=4.5V

13 AC Electrical Characteristics

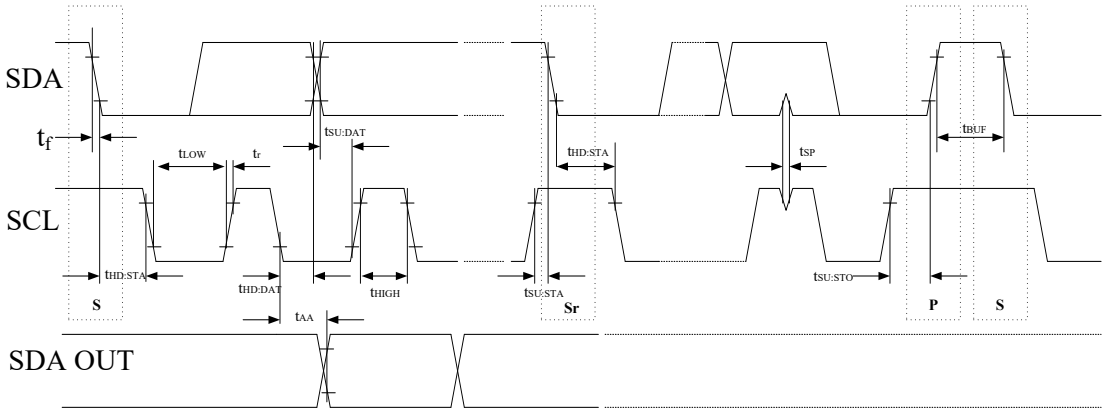
Frame Frequency

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD Frame Frequency	fLCD1	72	80	88	Hz	4.0V	1/4 duty,25℃
LCD Frame Frequency	fLCD2	144	160	176	Hz	4.0V	1/4 duty,25℃
LCD Frame Frequency	fLCD3	52	80	124	Hz	4.0V	1/4 duty,-40 ~ +85℃
LCD Frame Frequency	fLCD4	104	160	248	Hz	4.0V	1/4 duty,-40 ~ +85℃

I2C parameter

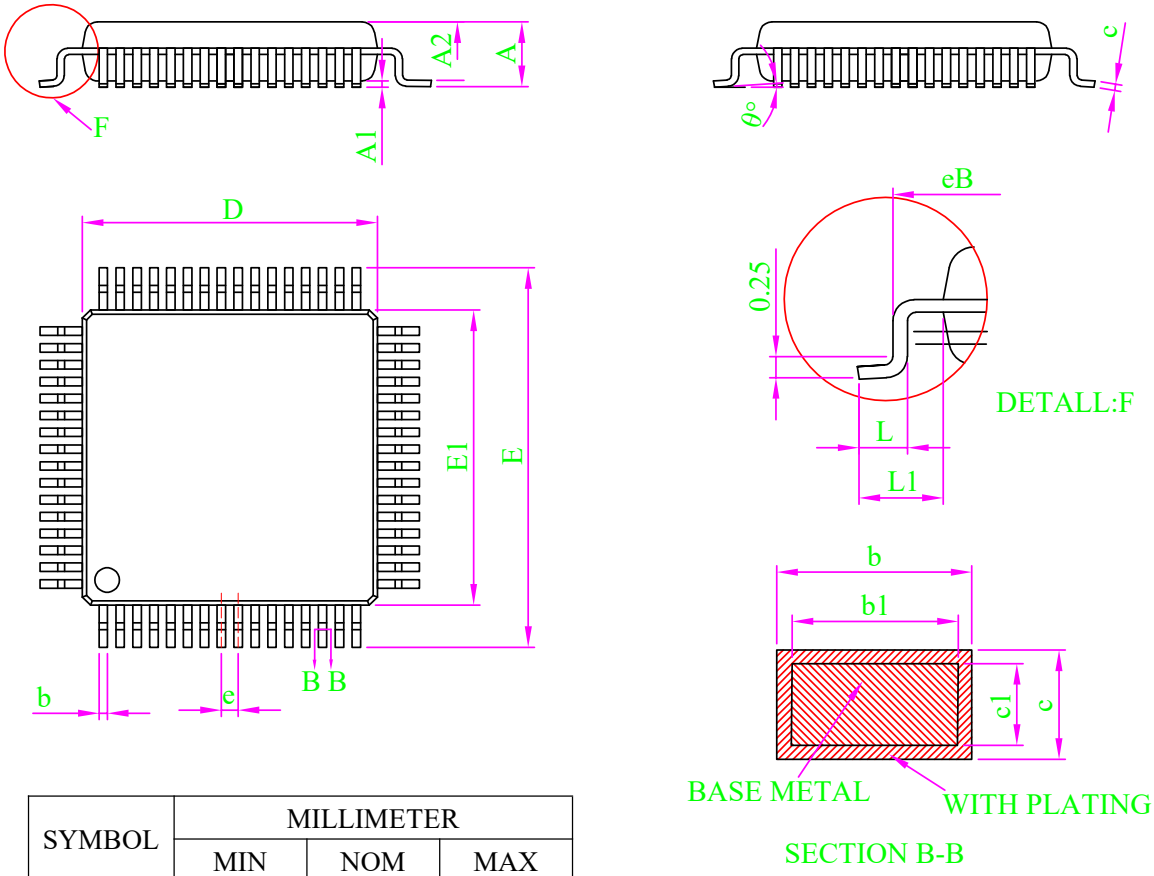
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	f_{SCL}	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	t_{BUF}	1.3	—	—	μs	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	$t_{HD:STA}$	0.6	—	—	μs	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	t_{LOW}	1.3	—	—	μs	3.0-5.5V	—
SCL High Time	t_{HIGH}	0.6	—	—	μs	3.0-5.5V	—
Start Condition Setup Time	$t_{SU:STA}$	0.6	—	—	μs	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	$t_{HD:DAT}$	0	—	—	ns	3.0-5.5V	—
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	t_R	—	—	0.3	μs	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	t_F	—	—	0.3	μs	3.0-5.5V	periodically sampled
Stop Condition Setup Time	$t_{SU:STO}$	0.6	—		μs	3.0-5.5V	—
Output Valid from Clock	t_{AA}	—	—	0.9	μs	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin)	t_{SP}	—	—	50	ns	3.0-5.5V	Noise suppression time

I^2C Timing


SDA
SCL
SDA OUT
tf
tLOW
tr
tSU:DAT
tHD:STA
tSP
tBUF
tHD:STA
tHD:DAT
tHIGH
tSU:STA
tSU:STO
tAA
S
Sr
P
S

14 Package Information

14.1 LQFP64 (7.0mm × 7.0mm PP=0.4mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.28
e	0.40 BSC		
L	0.42	0.57	0.72
L1	0.95	1.00	1.15
θ	0	-	10°

Note:

1. All dimension are in mm.
2. Dim D&El does not include plastic flash; Flash:Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/ intrusion.
4. Plating thickness 0.007mm-0.015mm

15 Disclaimer

Warranty and liability —— The information provided in this document is believed to be accurate and reliable. However, Shenzhen Vinka Microelectronics Co., Ltd. (hereinafter "the Company") makes no warranties, express or implied, as to the completeness or suitability of this information for any specific purpose.

In no event shall the Company be liable for any indirect, incidental, or consequential damages, including but not limited to loss of profits, equipment damage, or system failure, arising out of the use of this product or documentation, regardless of the legal theory under which such liability is asserted.

Right to change —— The Company reserves the right to modify any information contained herein without prior notice. The latest version of this document is available at: https://www.szvinka.com/

Applicability —— This product is not designed or intended for use in life-critical, medical, or safety systems where failure could result in injury or death. The customer shall assume full responsibility for any such use.

Application —— All product application descriptions provided herein are intended for illustrative purposes only.
The Company makes no representations or warranties, express or implied, regarding the suitability of any specific application without further testing or modification.

The customer is solely responsible for determining whether the Company's products are appropriate for their intended applications or end customers.

The customer shall ensure proper design practices, implementation safeguards, and operational validation to minimize risks associated with product use.

The Company shall not be held liable for any defects, losses, costs, or damages arising from weaknesses or failures in the customer's own products or applications, or from the integration or use of third-party products.

Furthermore, the customer shall conduct all necessary testing and validation for any third-party deployment of the Company's products to avoid potential misuse or associated damages. The Company assumes no liability in this regard.

Commercial terms of sale —— Unless otherwise agreed in writing, sales of this product are subject to the Company's standard terms and conditions of sale. The Company expressly rejects the applicability of the customer's general terms and conditions.

Export control—— This product may be subject to applicable export control regulations. The customer is solely responsible for compliance with such regulations, including obtaining any necessary export licenses.

16 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2024-08-01	Change Description	YES
5	1.4	2025-08-04	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/