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Vinka Microelectronics

VK1622S Datasheet

32×8 LCD DRIVER

Rev.1.3

1 General Description

The VK1622S is a RAM-mapped LCD segment driver capable of supporting up to 256 segments (32 SEG × 8 COM).
The device communication via a 3-wire or 4-wire serial interface, which is used for display parameter configuration, data transmission, and Power-down control.

2 Key Features

- Operating voltage:2.4-5.2V
- Integrated RC oscillator (default)
- External crystal input: 32.768 kHz (OSCI)
- Selectable LCD bias: 1/4
- Selectable LCD duty:1/8
- Built-in 32×8 bit display RAM
- Configurable buzzer output: 2 kHz or 4 kHz
- Power-down mode via software command(LCD OFF, SYS DIS)
- Eight selectable clock sources for time base / WDT
- WDT or time base overflow flag output via /IRQ pin
- 3 wire or 4 wire serial communication interface
- Software-configurable of LCD parameters
- Dual command formats for configuration and access
- Auto-increment addressing for sequential read/write
- Three RAM accessing modes
- VLCD adjustable via external pin (≤ VDD)
- Available Packages:
  LQFP44(10.0mm × 10.0mm PP=0.8mm)
  LQFP52(14.0mm×14.0mm PP=1.0mm)
  LQFP64(7.0mm×7.0mm PP=0.4mm)
  QFP64(20.0mm×14.0mm PP=1.0mm)
  DICE
  COG

3 Product Selection

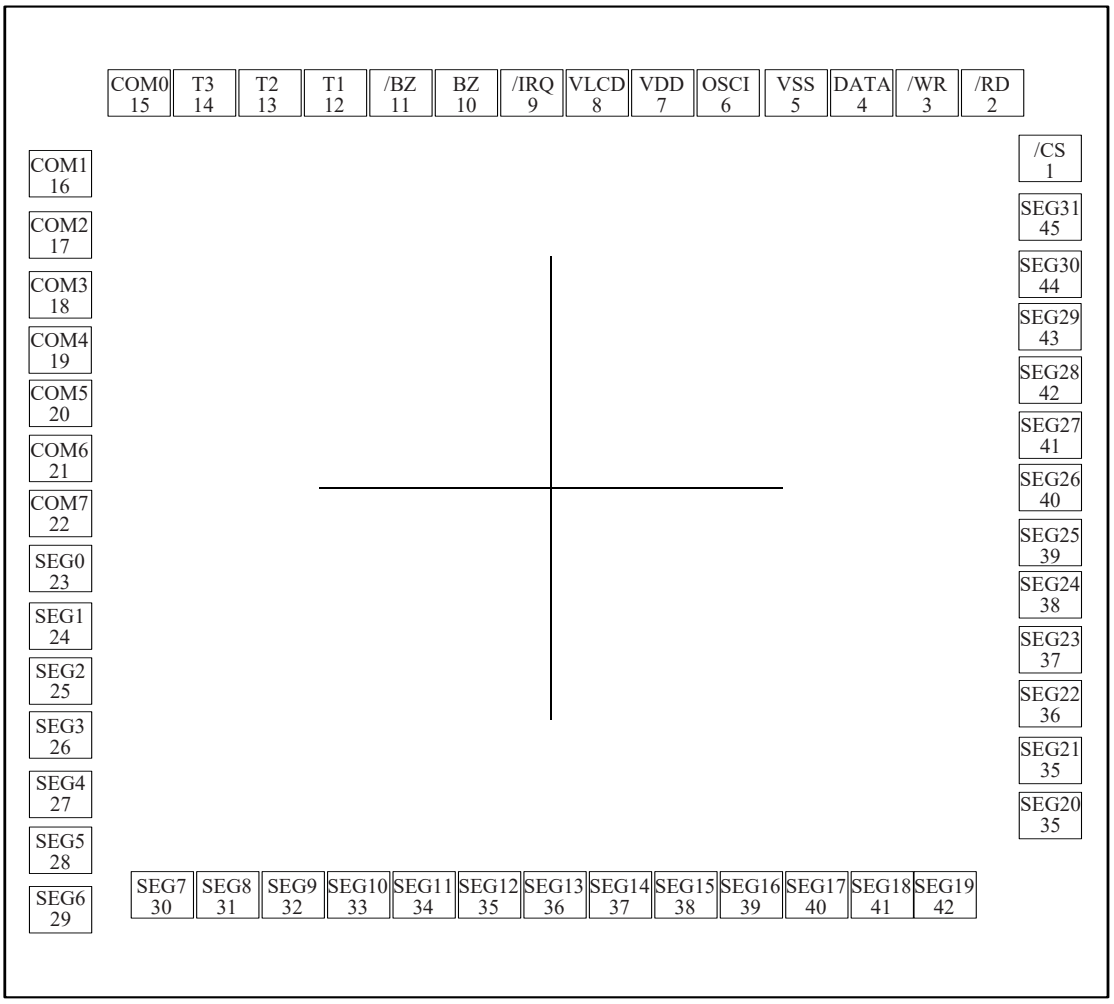
Part No.	VK1620	VK1621S-1	VK1622S	VK1623S	VK1625	VK1626
COM	4	4	8	8	8	16
SEG	32	32	32	48	64	48
On-chip Oscillator	-	√	√	√	√	√
Crystal Oscillator	√	√	-	√	√	√
External clock	√	√	√	√	√	√

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray Qty	Box Qty	Total Qty	Notes
VK1620	LQFP64		250/tray	2500/box	15000 PCS	
	DICE		300/tray	1500/box	3000 PCS	DICE
VK1621S-1	LQFP44		160/tray	1600/box	9600 PCS	
	LQFP48		250/tray	2500/box	15000 PCS	
	SSPO48	30/tube		2400/box	24000 PCS	
	DICE		300/tray	1500/box	3000 PCS	DICE
VK1622S	LQFP44		160/tray	1600/box	5400 PCS	
	LQFP52		90/tray	900/box	5400 PCS	
	LQFP64		250/tray	2500/box	15000 PCS	
	QFP64		66/tray	660/box	3960 PCS	
	DICE		250/tray	1000/box	2000 PCS	DICE
VK1623S	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		100/tray	500/box	1000 PCS	DICE
VK1625	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		100/tray	500/box	1000 PCS	DICE
VK1626	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		110/tray	550/box	1500 PCS	DICE

5 COB Pad Information

5.1 COB Pad Assignment



Chip Dimensions: 2080×1895 μm², substrate potential: VDD

Pad size: 90×90 μm, Pad spacing: 112 μm,

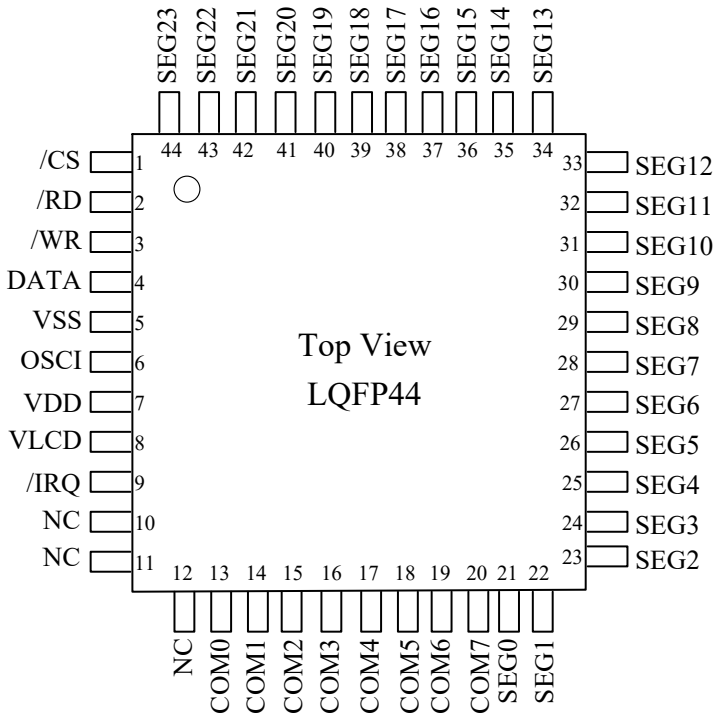
Al Pad size: 100×100μm, Al pad thickness: 1μm,

5.2 COB PAD Coordinates

Unit: um

Pad No	Name	X	Y	Pad No	Name	X	Y
1	/CS	885	646.9	28	SEG5	-885	-701.8
2	/RD	730.2	792.5	29	SEG6	-885	-811.8
3	/WR	620.2	792.5	30	SEG7	-603.1	-792.5
4	DATA	494.1	792.5	31	SEG8	-493.1	-792.5
5	VSS	377.1	792.5	32	SEG9	-383.1	-792.5
6	OSCI	267.1	792.5	33	SEG10	-273.1	-792.5
7	VDD	157.1	792.5	34	SEG11	-163.1	-792.5
8	VLCD	47.1	792.5	35	SEG12	-53.1	-792.5
9	/IRQ	-63.5	792.5	36	SEG13	56.9	-792.5
10	BZ	-185.8	792.5	37	SEG14	166.9	-792.5
11	/BZ	-312.9	792.5	38	SEG15	276.9	-792.5
12	T1	-433.2	792.5	39	SEG16	386.9	-792.5
13	T2	-543.2	792.5	40	SEG17	496.9	-792.5
14	T3	-653.2	792.5	41	SEG18	606.9	-792.5
15	COM0	-763.2	792.5	42	SEG19	716.9	-792.5
16	COM1	-885	618.2	43	SEG20	885	-673.1
17	COM2	-885	508.2	44	SEG21	885	-563.1
18	COM3	-885	398.2	45	SEG22	885	-453.1
19	COM4	-885	288.2	46	SEG23	885	-343.1
20	COM5	-885	178.2	47	SEG24	885	-233.1
21	COM6	-885	68.2	48	SEG25	885	-123.1
22	COM7	-885	-41.8	49	SEG26	885	-13.1
23	SEG0	-885	-151.8	50	SEG27	885	96.9
24	SEG1	-885	-261.8	51	SEG28	885	206.9
25	SEG2	-885	-371.8	52	SEG29	885	316.9
26	SEG3	-885	-481.8	53	SEG30	885	426.9
27	SEG4	-885	-591.8	54	SEG31	885	536.9

6 Package Pinout Information(LQFP44)

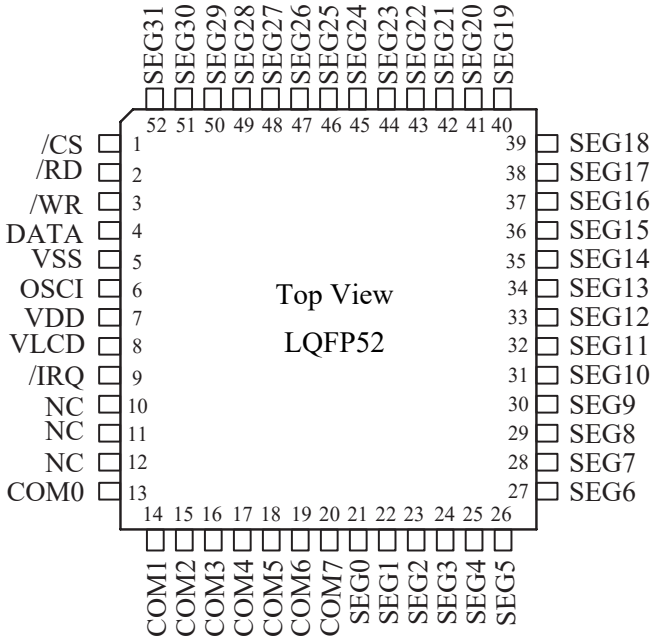


For more information: Page 27

6.1 VK1622S/LQFP44 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip select signal with pull-up resistor ,active low.
2	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
3	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
4	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
5	VSS	VSS	Negative power suppl
6	OSCI	I	External clock source: OSCI connect a external clock source
7	VDD	VDD	Positive power supply
8	VLCD	I	LCD driving voltage input,must be ≤VDD
9	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
10-12	NC	—	——
13-20	COM0-COM7	O	LCD COM drive outputs
21-44	SEG0-SEG23	O	LCD SEG drive outputs

7 Package Pinout Information(LQFP52)

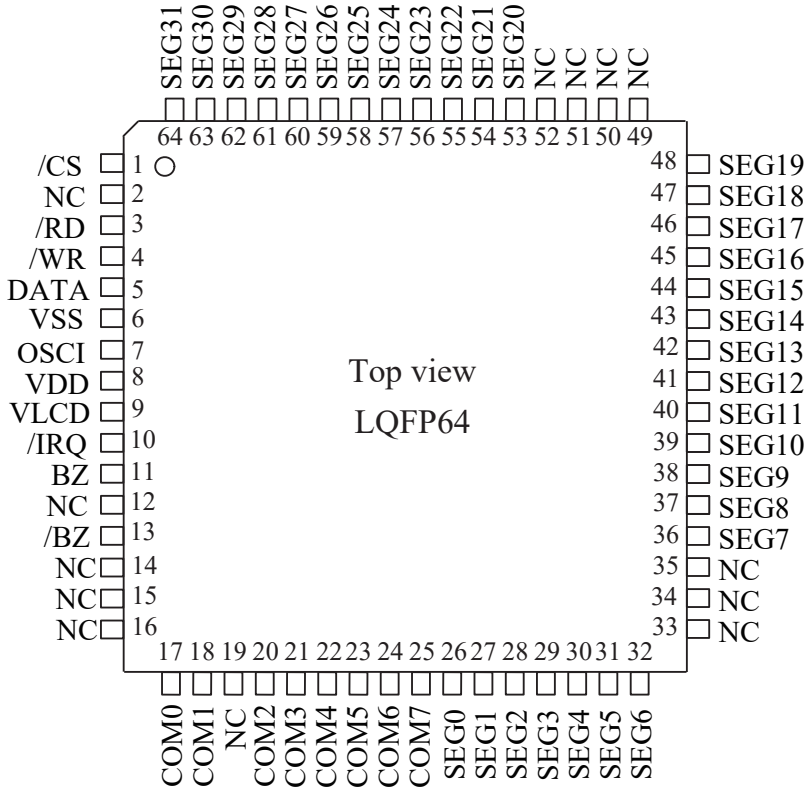


For more information: Page 28

7.1 VK1622S/LQFP52 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip select signal with pull-up resistor ,active low.
2	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
3	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
4	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
5	VSS	VSS	Negative power supply
6	OSCI	I	External clock source: OSCI connect a external clock source
7	VDD	VDD	Positive power supply
8	VLCD	I	LCD driving voltage input,must be ≤VDD
9	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
10-12	NC	—	——
13-20	COM0-COM7	O	LCD COM drive outputs
21-52	SEG0-SEG31	O	LCD SEG drive outputs

8 Package Pinout Information(LQFP64)

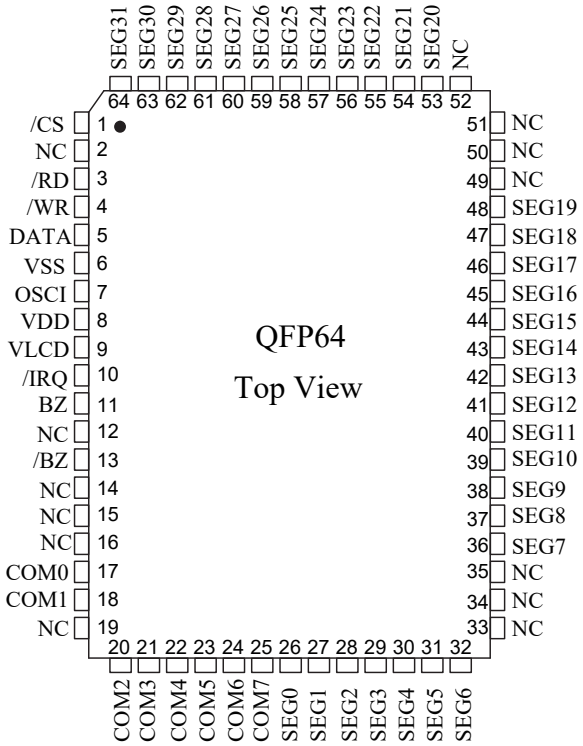


For more information: Page 29

8.1 VK1622S/LQFP64 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip select signal with pull-up resistor ,active low.
3	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
4	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
5	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
6	VSS	VSS	Negative power supply
7	OSCI	I	External clock source: OSCI connect a external clock source
8	VDD	VDD	Positive power supply
9	VLCD	I	LCD driving voltage input,must be ≤VDD
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output， when TONE OFF the /BZ pin output low level.
13	/BZ	O	
14-16	NC	—	——
17,18 20-25	COM0-COM7	O	LCD COM drive outputs
26-32 36-48 53-64	SEG0-SEG31	O	LCD SEG drive outputs

9 Package Pinout Information(QFP64)



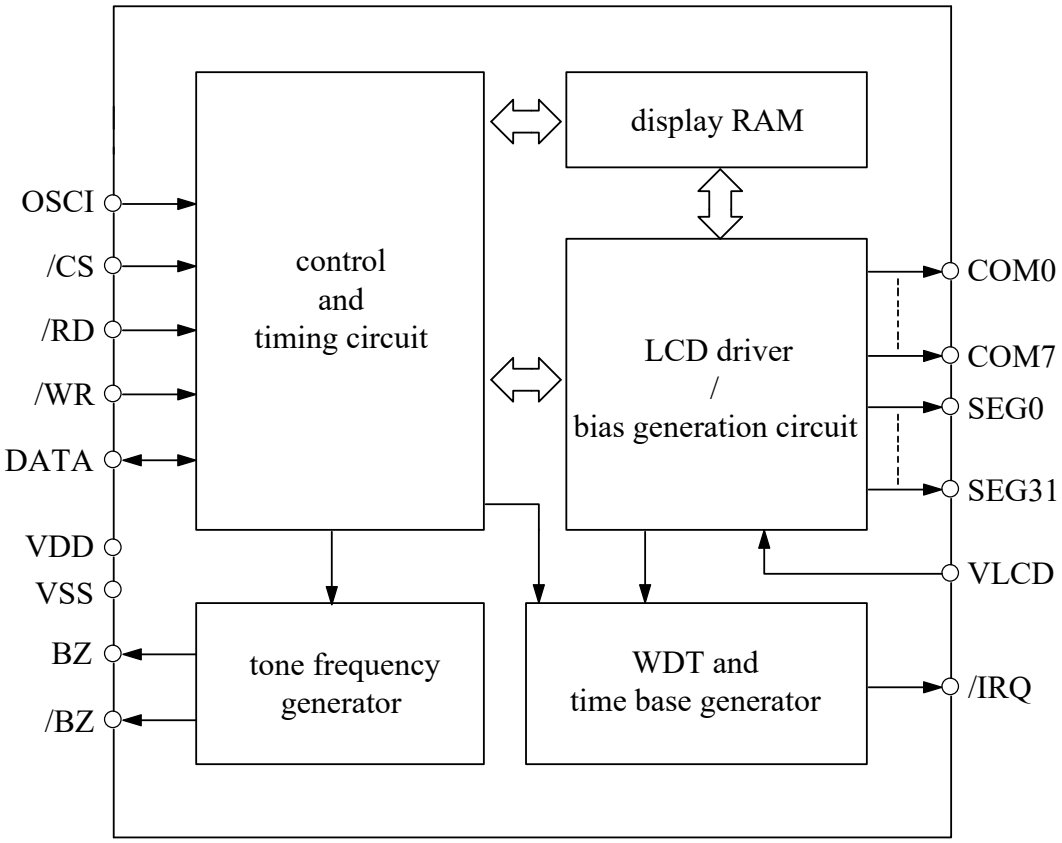
For more information: Page 30

9.1 VK1622S/QFP64 Pin Description

No.	Name	I/O	Function
1	/CS	I	Chip select signal with pull-up resistor ,active low.
3	/RD	I	Serial read signal with pull-up resistor, data out on the falling edge of the /RD signal.
4	/WR	I	Serial write signal with pull-up resistor, data latched on the rising edge of the /WR signal.
5	DATA	I/O	Serial data signal with pull-up resistor, input/output depending on access mode.
6	VSS	VSS	Negative power supply
7	OSCI	I	External clock source: OSCI connect a external clock source
8	VDD	VDD	Positive power supply
9	VLCD	I	LCD driving voltage input,must be ≤VDD
10	/IRQ	O	Time base or WDT overflow flag, NMOS open drain output.
11	BZ	O	2kHz or 4kHz tone frequency output， when TONE OFF the /BZ pin output low level.
13	/BZ	O	
14-16	NC	—	——
17,18 20-25	COM0-COM7	O	LCD COM drive outputs
26-32 36-48 53-64	SEG0-SEG31	O	LCD SEG drive outputs

10 Functional Description

10.1 Block Diagram



10.2 Display RAM

The VK1622S integrates 32 × 8-bit RAM for LCD display. directly mapped to SEGx/COMx segments. Data is latched and updated on the LCD according to scan timing set by the system configuration. The display RAM can be accessed using three commands: READ, WRITE, and READ-MODIFY-WRITE. Each RAM address corresponds to a specific combination of SEG and COM lines.

The following is a mapping from the RAM to the LCD pattern:

	COM7	COM6	COM5	COM4		COM3	COM2	COM1	COM0		
SEG0					1					0	address 6 bit （A5----A0）
SEG1					3					2	
SEG2					5					4	
SEG3					7					6	
⋮					⋮					⋮	
SEG31					63					62	
	D3	D2	D1	D0	Data\Addr	D3	D2	D1	D0	Data\Addr	

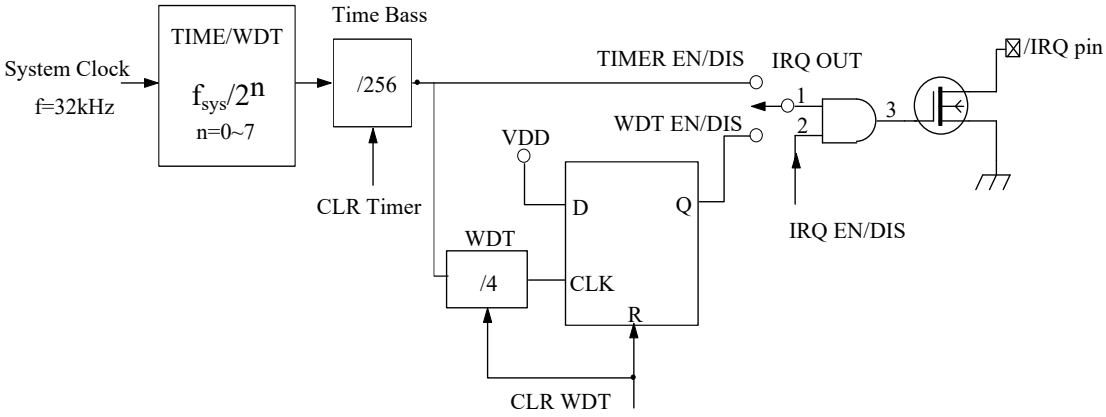
10.3 Time Base and WDT

The time base generator consists of an 8-stage ripple counter and provides accurate timing functionality. The Watchdog Timer (WDT) comprises the 8-stage time base plus an additional 2-stage counter. It helps reset or interrupt the host system in case of abnormal operation, such as unexpected jumps or execution errors. A WDT timeout sets an internal status flag. Both the time base overflow and WDT timeout flags can be routed to the /IRQ pin through software configuration. Eight frequency division options are available for the time base and WDT clock, derived using the formula:

$$f_{WDT}=fsys/2^{n} \quad (n=0\sim7) \quad fsys=32kHz$$

The time base generator and the Watchdog Timer (WDT) share the same 8-stage counter. The WDT is cleared by executing the CLR WDT command, while the time base generator can be cleared using either the CLR WDT or the CLR TIMER command. Executing the WDT EN command enables both the time base generator and the WDT timeout flag output, which can be routed to the /IRQ pin. Conversely, executing the WDT DIS command disables the time base generator. After the TIMER EN command is issued, the WDT is disconnected from the /IRQ pin, and the time base overflow signal is instead connected to it. The /IRQ output can be globally enabled or disabled using the IRQ EN and IRQ DIS commands, respectively.By default, the /IRQ output is disabled upon system power-up

Timer and WDT Configurations：



10.4 Tone Output

The VK1622S integrates a basic tone generator capable of producing 2 kHz or 4 kHz output signals. The output consists of a differential pair: BZ and /BZ, designed to drive a passive piezoelectric buzzer. Use the TONE 2K or TONE 4K commands to select the desired tone frequency. Tone output can be enabled or disabled via the TONE ON or TONE OFF commands. When the tone function is disabled or the system is powered down, both BZ and /BZ will remain at low level.

10.5 LCD Driver

The VK1622S is a 256-segment LCD driver (32 SEG × 8 COM). It supports software configurable bias settings of 1/4, and COM configurations of 8.

10.6 Communication Interfacing

The VK1622S communicates with the host via a 3-wire or 4-wire serial interface.

When used solely for display output, only 3 lines are required (/CS, /WR, and DATA); /RD is optional for reading.

- /CS: Chip select input. It enables the serial interface when low and terminates communication when high.
- /RD: Read clock input. On the falling edge, data is output from the device onto the DATA line.
- /WR: Write clock input. On the rising edge, data and commands from DATA are latched into the device.
- DATA: Bidirectional serial data line used to transfer both command and display data.
- /IRQ: Open-drain output pin for either WDT timeout or time base overflow flag, selectable via software.

10.7 Command Format

The VK1622S is configured via software commands that support two primary modes: command mode and data mode.

- Command mode is used to configure system-level parameters. It is identified by a command mode ID of 100.
- Data mode supports three types of memory operations: READ, WRITE, and READ-MODIFY-WRITE.

These commands allow the host controller to configure LCD behavior and access display RAM contents.

The following are the data mode IDs and the command mode ID:

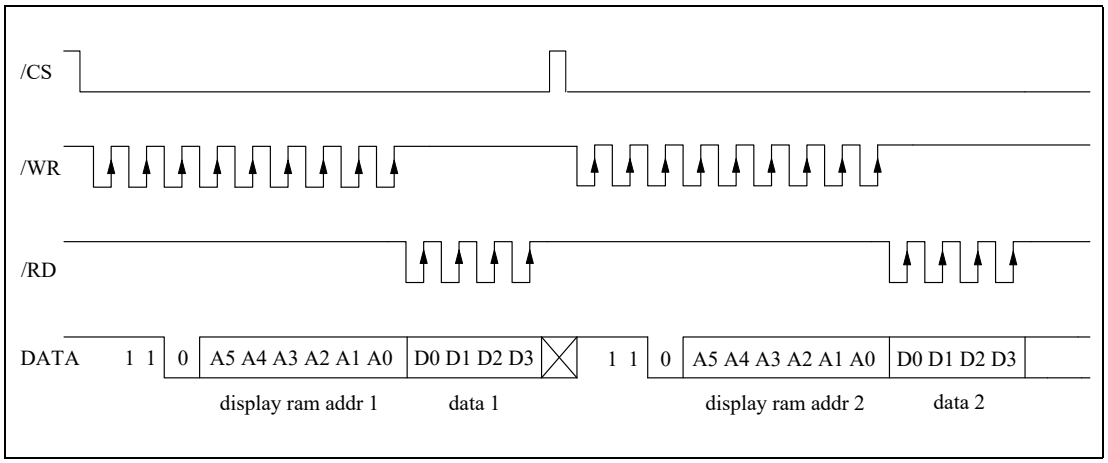
Command	MODE	ID
READ	DATA	110
WRITE	DATA	101
Read-Modify-Write	DATA	101
COMMAND	COMMAND	100

11 Cmd/Data Timing Diagram

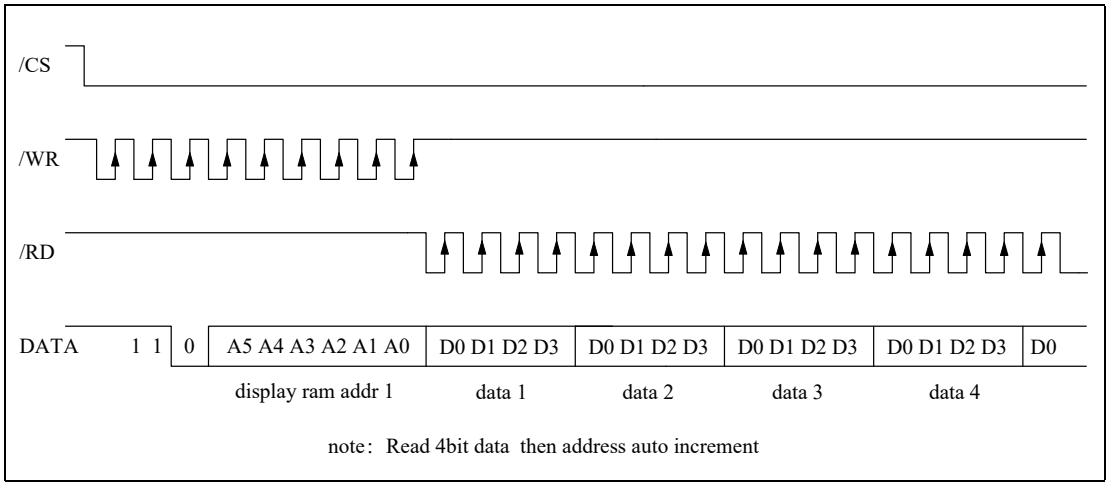
The following are the data mode IDs and the command mode ID Timing Diagrams.

11.1 READ Mode

Command Code : 110

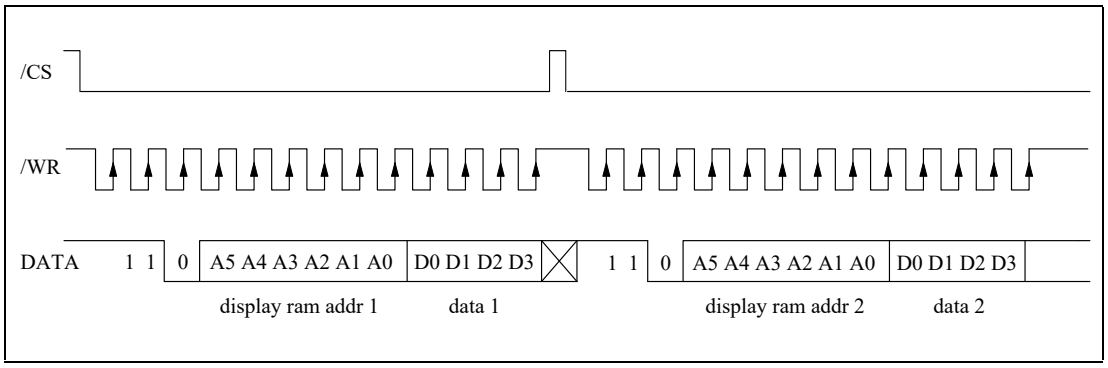


Successive Address Reading

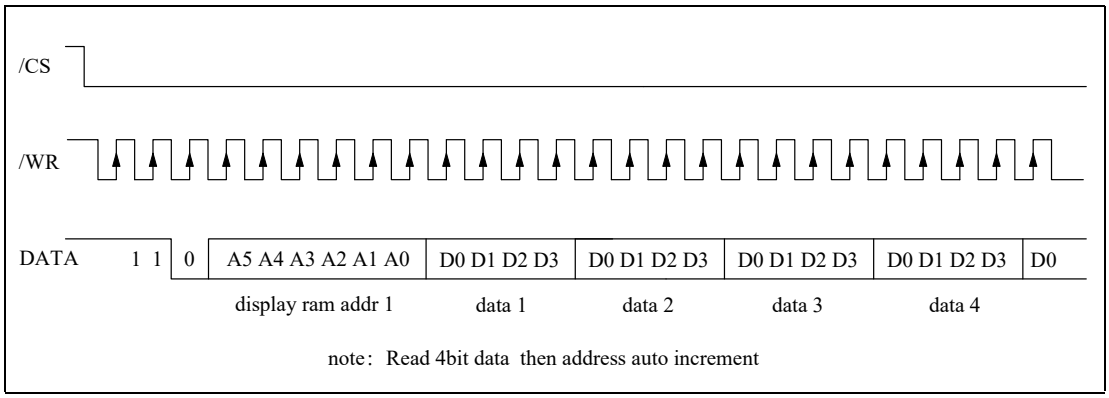


11.2 WRITE Mode

Command Code : 101

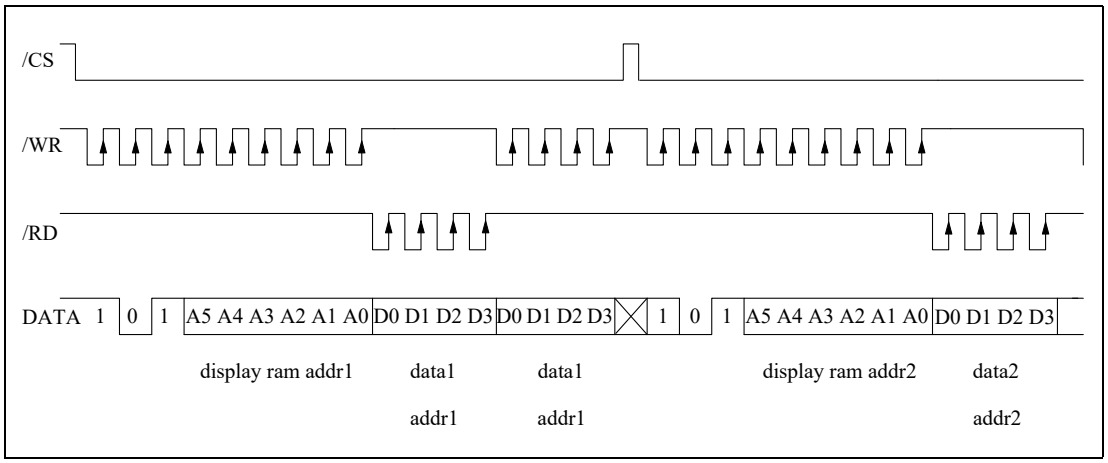


Successive Address Writing

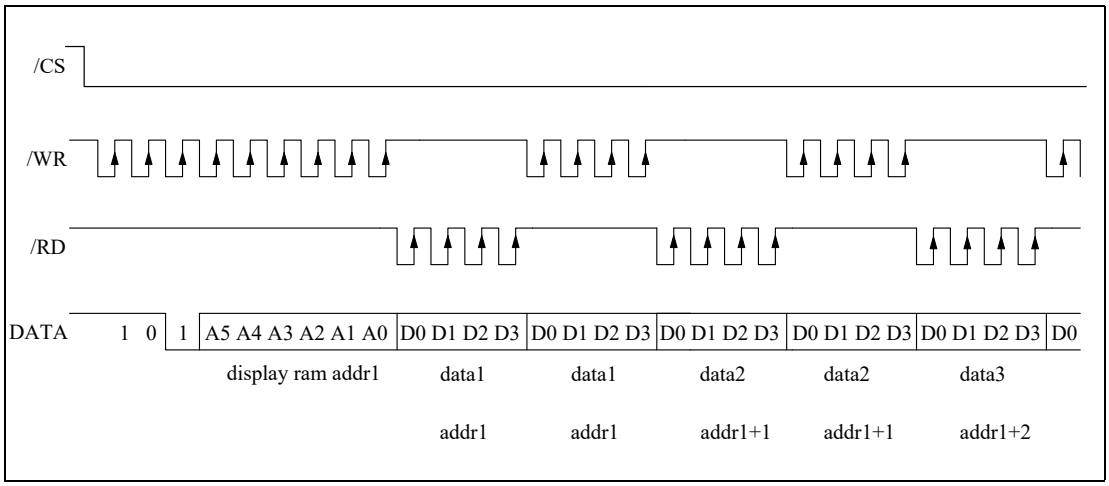


11.3 Read-Modify-Write Mode

Command Code : 101

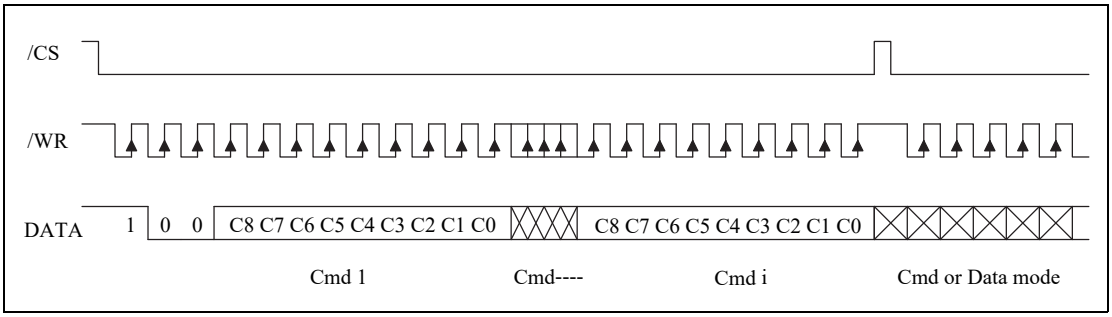


Successive Address Accessing



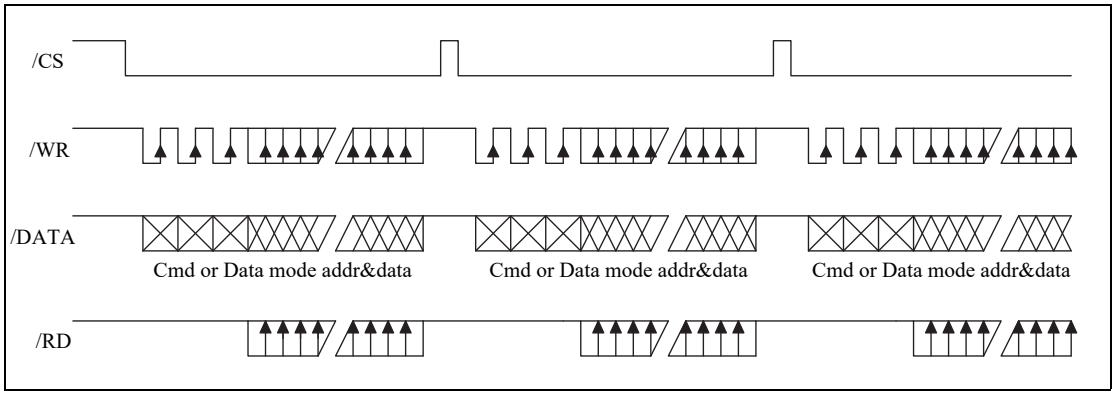
11.4 Command Mode

Command Code : 100



11.5 Data and Command Mode

Data and Command Mode



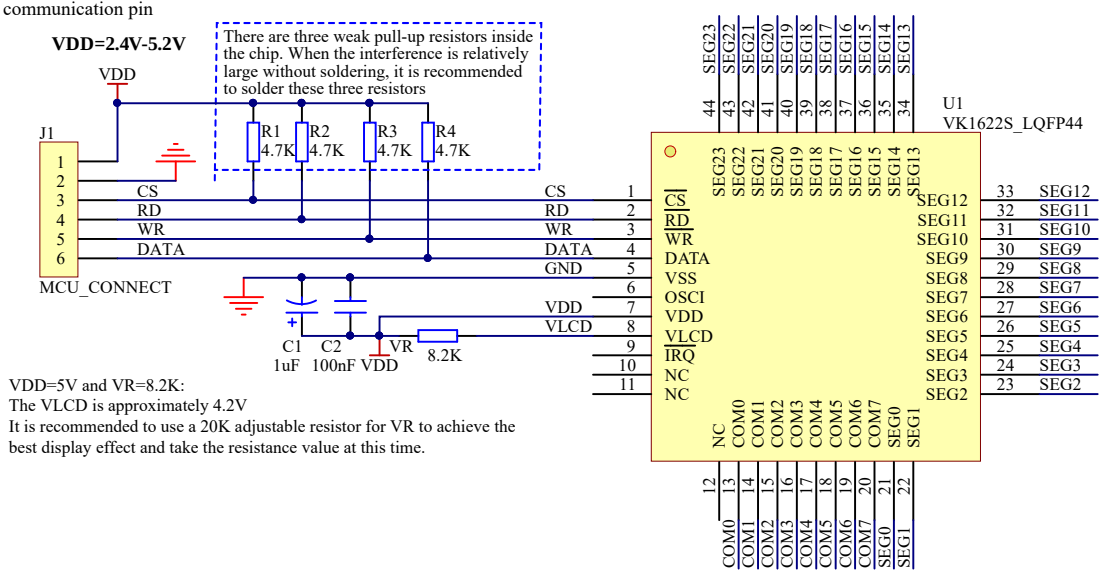
12 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off both system oscillator	YES
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
TIMERS DIS	100	0000-0100-X	C	Disable time base output	
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag output	
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	YES
CLR TIMER	100	0000-11XX-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
RC 32k	100	0001-10XX-X	C	on-chip RC oscillator	YES
EXT 32k	100	0001-11XX-X	C	external clock source	
TONE 4k	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2k	100	011X-XXXX-X	C	Tone frequency, 2kHz	
IRQ DIS	100	100X-0XXX-X	C	Disable IRQ output	YES
IRQ EN	100	100X-1XXX-X	C	Enable IRQ output	
F1	100	101X-X000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	100	101X-X001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	100	101X-X010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	
F8	100	101X-X011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-X100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-X101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-X110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-X111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	YES
TEST	100	1110-0000-X	C	Test mode	
NORMAL	100	1110-0011-X	C	Normal mode	YES

note: X: 0 or 1 D/C:Data/Command mode
A5-A0: Display RAM addresses Def.:Power on reset default
D3-D0:4bit Display RAM data 110,101and 100 is Command ID

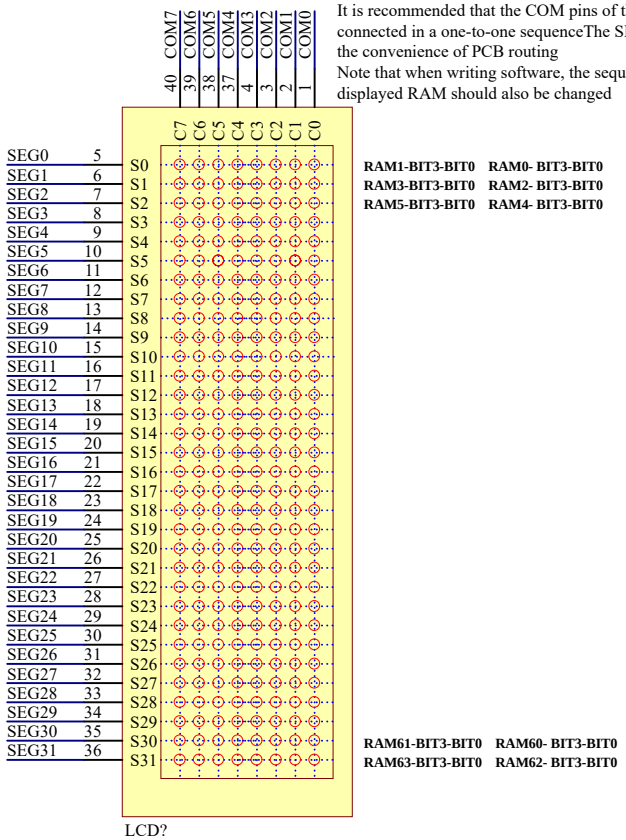
13 Application Circuits

When the surrounding interference is relatively large, a 10R to 1k resistor and a small PF-level capacitor to ground can be connected in series on the communication pin
When the power supply of the chip machine (3.3V) and the driver chip (5V) is inconsistent, it is recommended to add a level conversion circuit to the communication pin

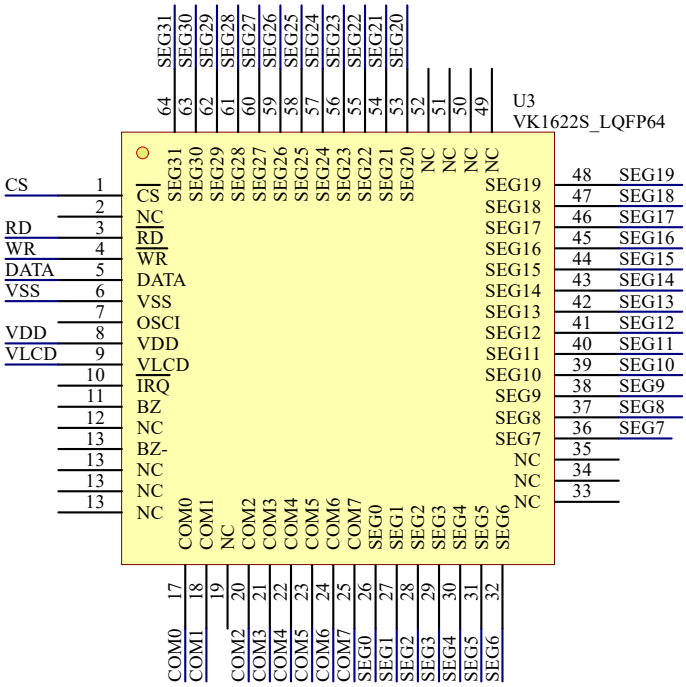


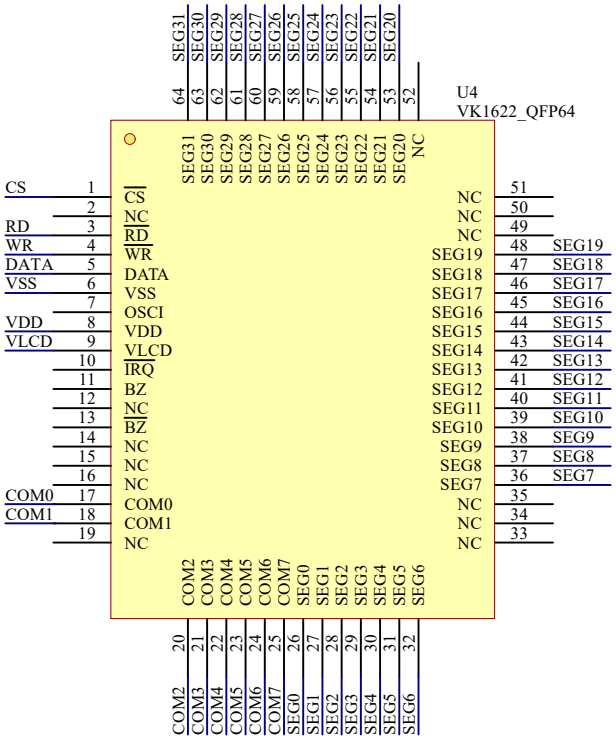
VDD=5V and VR=8.2K:
The VLCD is approximately 4.2V
It is recommended to use a 20K adjustable resistor for VR to achieve the best display effect and take the resistance value at this time.

It is recommended that the COM pins of the chip and the LCD be connected in a one-to-one sequenceThe SEG pins can be shuffled for the convenience of PCB routing
Note that when writing software, the sequence corresponding to the displayed RAM should also be changed



LCD?
LCD SEG32xCOM8


U3
VK1622S_LQFP64
CS 1
NC 2
RD 3
WR 4
DATA 5
VSS 6
7
VDD 8
VLCD 9
10
IRQ
BZ 11
NC 12
BZ- 13
NC 13
NC 13
NC 13
SEG19 48
SEG18 47
SEG17 46
SEG16 45
SEG15 44
SEG14 43
SEG13 42
SEG12 41
SEG11 40
SEG10 39
SEG9 38
SEG8 37
SEG7 36
NC 35
NC 34
NC 33
COM0 17
COM1 18
19 NC
COM2 20
COM3 21
COM4 22
COM5 23
COM6 24
COM7 25
SEG0 26
SEG1 27
SEG2 28
SEG3 29
SEG4 30
SEG5 31
SEG6 32
64 SEG31
63 SEG30
62 SEG29
61 SEG28
60 SEG27
59 SEG26
58 SEG25
57 SEG24
56 SEG23
55 SEG22
54 SEG21
53 SEG20
52 NC
51 NC
50 NC
49 NC


U4
VK1622_QFP64
CS 1
RD 3
WR 4
DATA 5
VSS 6
7
VDD 8
VLCD 9
10
11
12
13
14
15
16
COM0 17
COM1 18
19 NC
NC 51
NC 50
NC 49
SEG19 48
SEG18 47
SEG17 46
SEG16 45
SEG15 44
SEG14 43
SEG13 42
SEG12 41
SEG11 40
SEG10 39
SEG9 38
SEG8 37
SEG7 36
NC 35
NC 34
NC 33
COM2 20
COM3 21
COM4 22
COM5 23
COM6 24
COM7 25
SEG0 26
SEG1 27
SEG2 28
SEG3 29
SEG4 30
SEG5 31
SEG6 32
64 SEG31
63 SEG30
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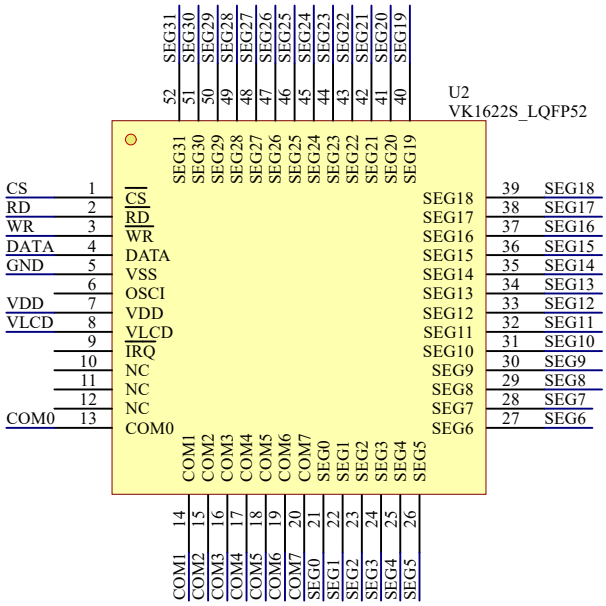
53 SEG20
52 NC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VK1622S_LQFP52
CS 1
RD 2
WR 3
DATA 4
GND 5
6
VDD 7
VLCD 8
9
10
11
12
COM0 13
SEG18 39
SEG17 38
SEG16 37
SEG15 36
SEG14 35
SEG13 34
SEG12 33
SEG11 32
SEG10 31
SEG9 30
SEG8 29
SEG7 28
SEG6 27
COM1 14
COM2 15
COM3 16
COM4 17
COM5 18
COM6 19
COM7 20
SEG0 21
SEG1 22
SEG2 23
SEG3 24
SEG4 25
SEG5 26
52 SEG31
51 SEG30
50 SEG29
49 SEG28
48 SEG27
47 SEG26
46 SEG25
45 SEG24
44 SEG23
43 SEG22
42 SEG21
41 SEG20
40 SEG19

14 Electrical Characteristics

14.1 Absolute Maximum Ratings

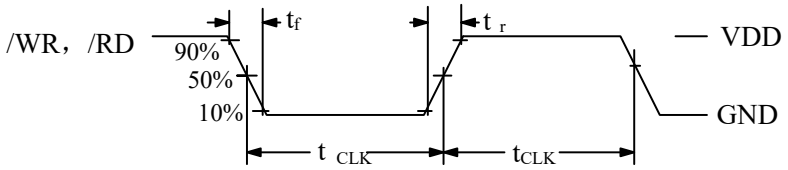
Parameter	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3～5.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	T_{STG}	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

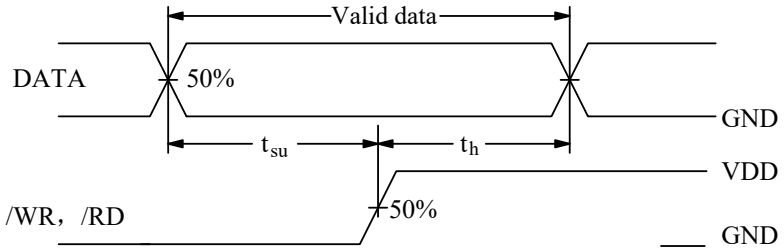
14.2 DC Electrical Characteristics

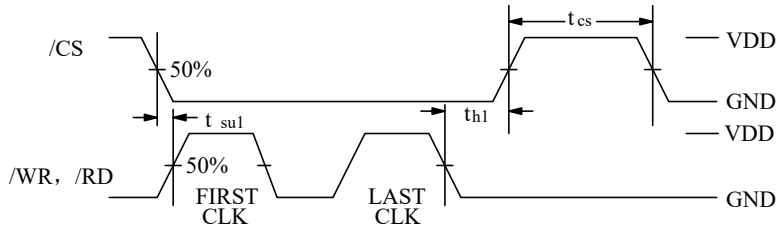
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	I_{DD1}	—	80	210	μA	3V	No load/LCD ON On-chip RC oscillator
		—	135	415		5V	
Operating current	I_{DD2}	—	8	30	μA	3V	No load/LCD OFF On-chip RC oscillator
		—	20	55		5V	
Standby Current	I_{STB}	—	1	8	μA	3V	No load, Power down mode
		—	2	16		5V	
Low-level Input	V_{IL}	0	—	0.6	V	3V	DATA, /WR, /CS,/RD
		0	—	1.0		5V	
High-level Input	V_{IH}	2.4	—	3.0	V	3V	DATA, /WR, /CS,/RD
		4.0	—	5.0		5V	
BZ, /BZ, /IRQ	I_{OL1}	0.9	1.8	—	mA	3V	V_{OL}=0.3V
		1.7	3.0	—		5V	V_{OL}=0.5V
BZ,/BZ	I_{OH1}	-0.9	-1.8	—	mA	3V	V_{OH}=2.7V
		-1.7	-3.0	—		5V	V_{OH}=4.5V
DATA	I_{OL1}	200	450	—	μA	3V	V_{OL}=0.3V
		250	500	—		5V	V_{OL}=0.5V
DATA	I_{OH1}	-200	-450	—	μA	3V	V_{OH}=2.7V
		-250	-500	—		5V	V_{OH}=4.5V
LCD COM Sink Current	I_{OL2}	15	40	—	μA	3V	V_{OL}=0.3V
		100	200	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH2}	-15	-30	—	μA	3V	V_{OH}=2.7V
		-45	-90	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL3}	15	30	—	μA	3V	V_{OL}=0.3V
		70	150	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH3}	-6	-13	—	μA	3V	V_{OH}=2.7V
		-20	-40	—		5V	V_{OH}=4.5V
Pull-UP Resistor	R_{UP}	100	200	300	kΩ	3V	DATA, /WR, /CS,/RD
		50	100	150		5V	

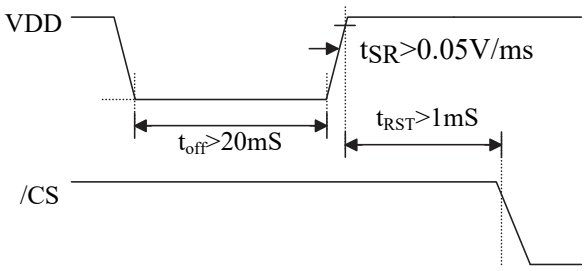
14.3 AC Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	22	32	40	kHz	3V	On-chip RC oscillator
		24	32	40		5V	
System Clock	f_{SYS2}	—	32	—	kHz	3V	External clock source
		—	32	—		5V	
LCD Clock	f_{LCD1}	44	64	80	Hz	3V	On-chip RC oscillator
		48	64	80	Hz	5V	
	f_{LCD2}	—	64	—	Hz	3V	External clock source
		—	64	—	Hz	5V	
LCD Common Period	t_{COM}	—	n/ f_{LCD}	—	sec	—	N:Number of COM
Serial Data Clock(/WR)	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Data Clock(/RD)	F_{CLK2}	—	—	75	kHz	3V	Duty cycle 50%
		—	—	150		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS
/WR, /RD Input Pulse Width	t_{CLK}	3.34	—	—	μs	3V	Write mode
		6.67	—	—			Read mode
		1.67	—	—	μs	5V	Write mode
		3.34	—	—			Read mode
Rise/Fall Time Serial Data Clock Width	t_r, t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR, /RD Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to /WR, /RD Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR, /RD Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to /WR, /RD Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	


/WR，/RD
90%
50%
10%
tf
t r
t CLK
tCLK
VDD
GND

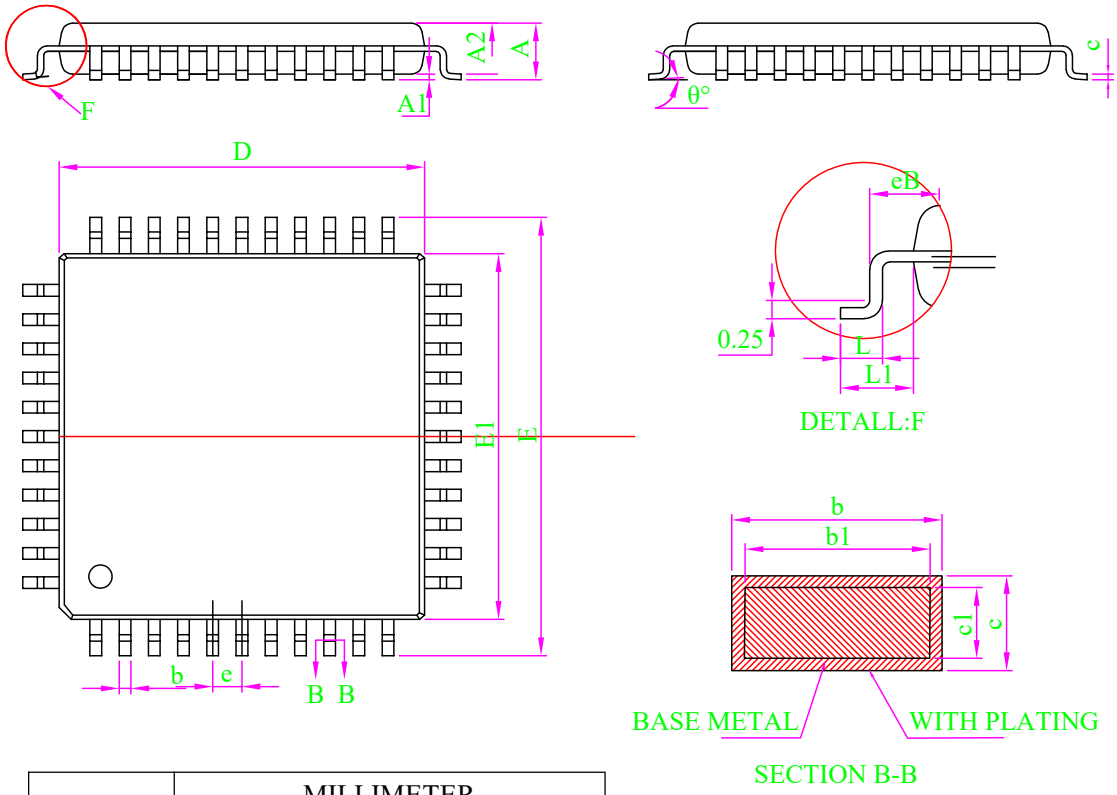

Valid data
DATA
50%
tsu
th
GND
VDD
/WR，/RD
50%
GND


/CS
50%
t cs
VDD
GND
t su1
th1
VDD
/WR，/RD
50%
FIRST CLK
LAST CLK
GND


VDD
tSR>0.05V/ms
toff>20mS
tRST>1mS
/CS

15 Package Information

15.1 LQFP44(10.0mm x 10.0mm PP=0.8mm)

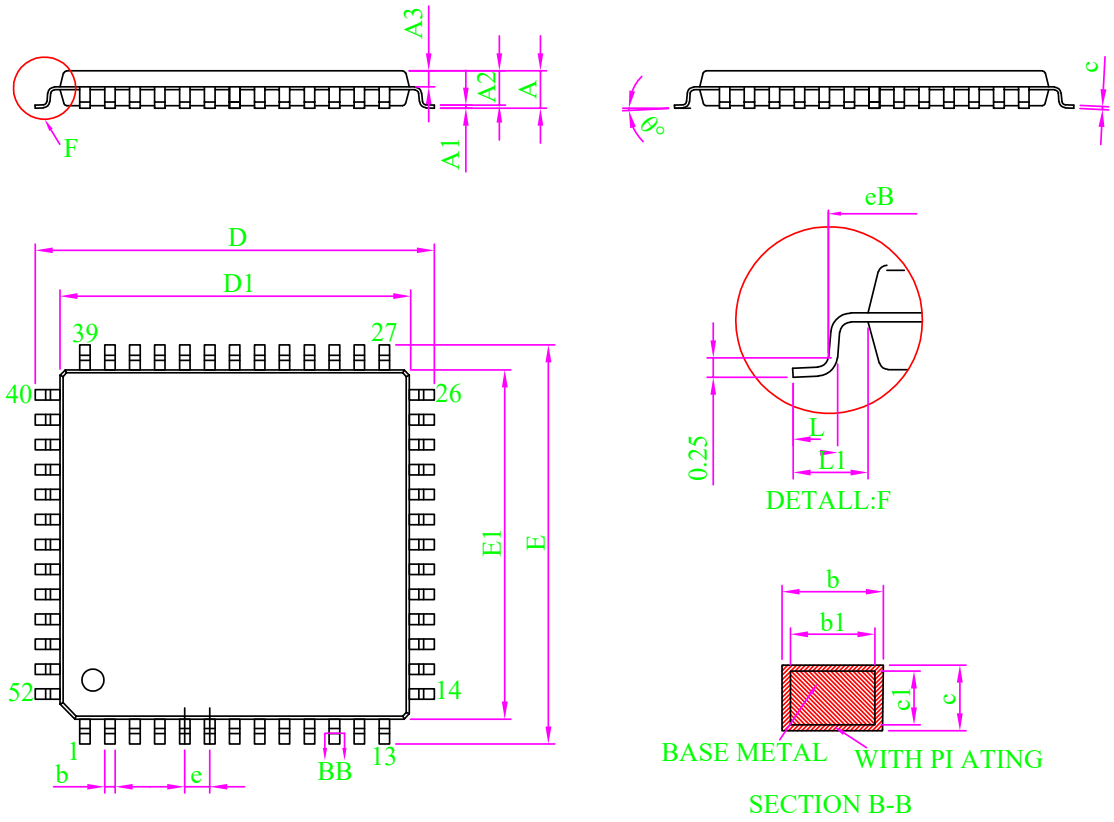


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
b	0.28	-	0.36
b1	0.27	0.30	0.33
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	9.90	10.00	10.10
E	11.80	12.00	12.20
eB	11.05	-	11.30
E1	9.90	10.00	10.10
e	0.80 BSC		
L	0.42	0.57	0.72
L1	0.95	1.00	1.15
θ	0	-	8°

Note:

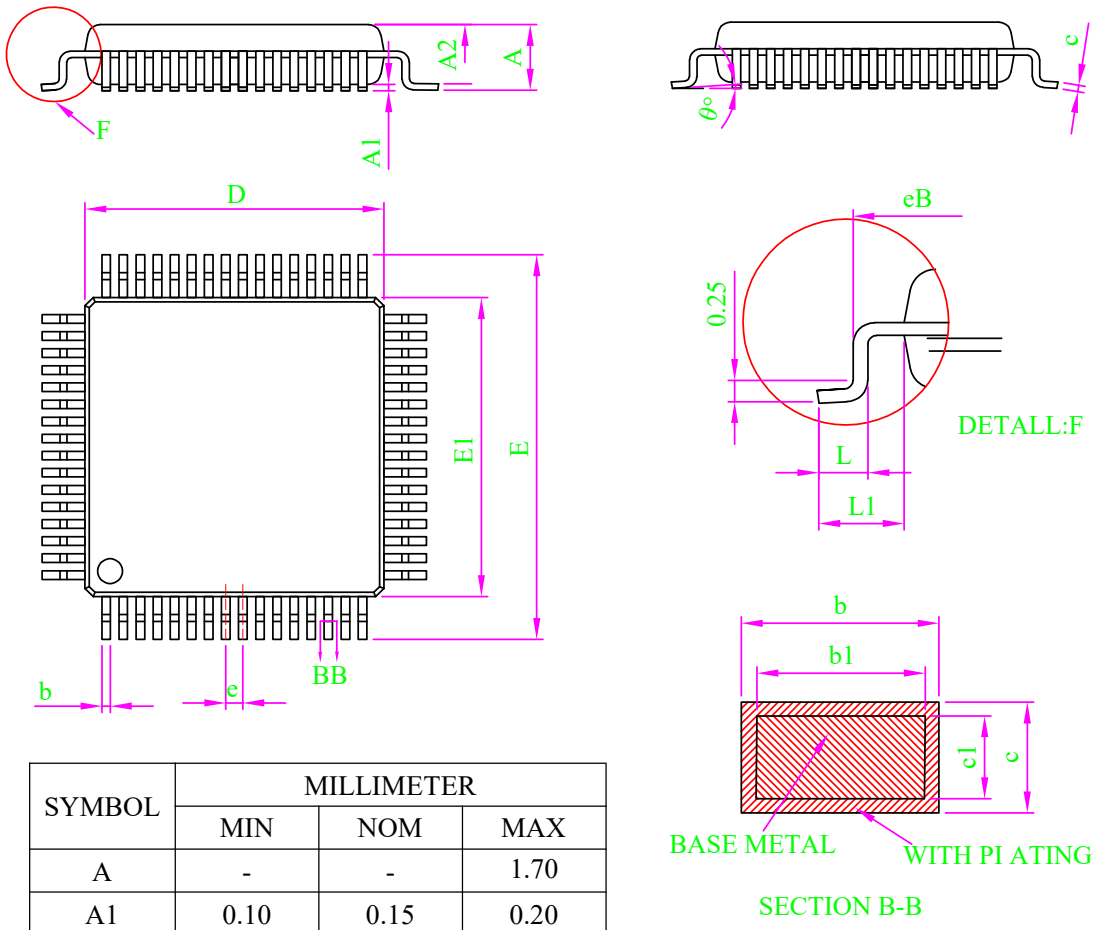
1. All dimension are in mm.
2. Dim D&El does not include plastic flash; Flash: Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.007mm-0.015mm

15.2 LQFP52（14.0mm × 14.0mm PP=1.0mm）



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.38	-	0.46
b1	0.37	0.40	0.43
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
eB	15.05	-	15.35
e	1.00 BSC		
L	0.45	-	0.75
L1	1.00 REF		
θ	0	-	7°

15.3 LQFP64（7.0mm × 7.0mm PP=0.4mm）

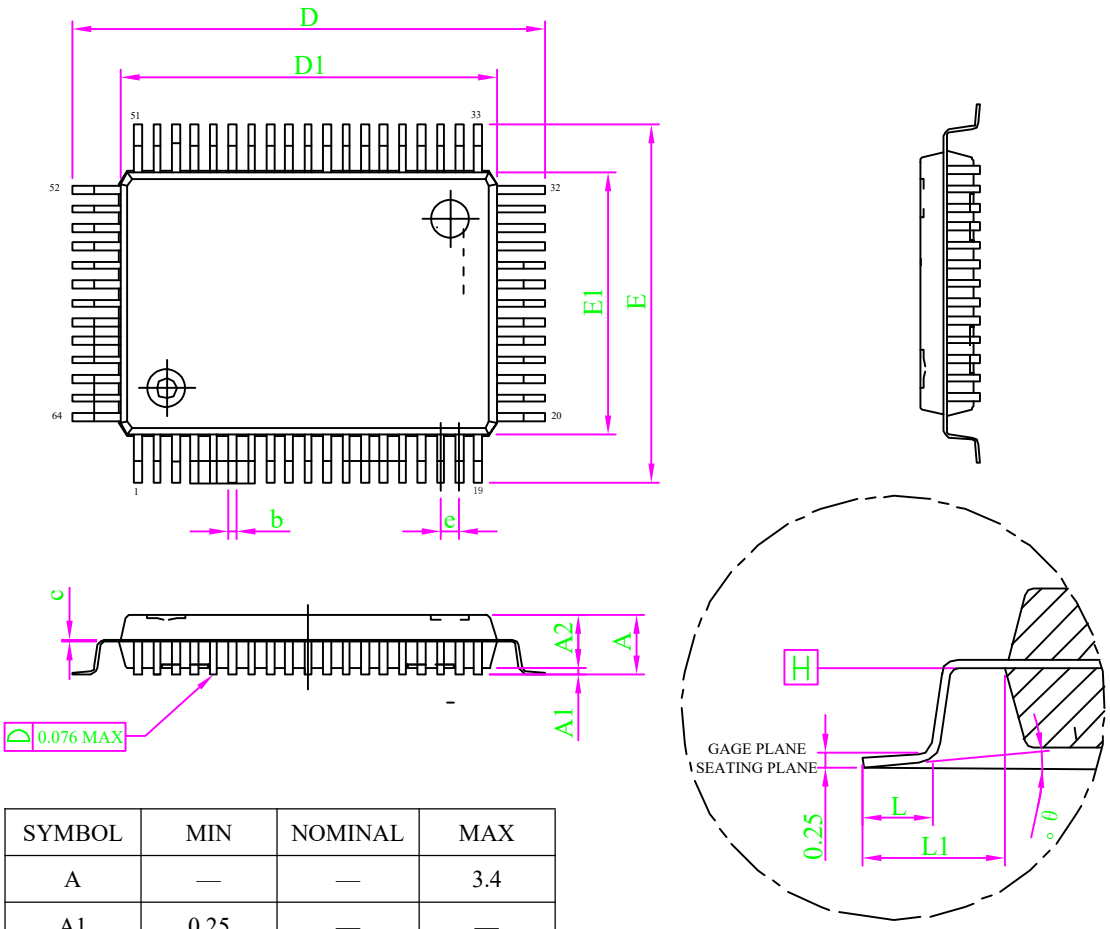


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.28
e	0.40 BSC		
L	0.42	0.57	0.72
L1	0.95	1.00	1.15
θ	0	-	10°

Note:

1. All dimension are in mm.
2. Dim D&El does not include plastic flash; Flash: Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.007mm-0.015mm

15.4 QFP64(20.0mm × 14.0mm PP=1.0mm)



SYMBOL	MIN	NOMINAL	MAX
A	—	—	3.4
A1	0.25	—	—
A2	2.55	2.72	3.05
b	0.35	0.40	0.50
c	0.11	0.15	0.23
D	25.00 BASIC		
D1	20.00 BASIC		
e	1.00 BASIC		
E	19.00 BASIC		
E1	14.00 BASIC		
L	1.15	1.30	1.45
L1	2.50REF		
θ°	0	3.5	7

UNIT： mm

NOTES：
1.JEDEC:N/A

2.DATUM PLANE H IS LOCATED THE BOTTOM OF THE MOLO PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BOOY.

3.DIMENSIONS D1 AND E1 D0 N INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDR. DIMENSIONS D1 AND E1 DD INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b DOES NOT INCLU DAMBAR PROTRUSION.

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17 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	initial release	YES
2	1.1	2018-10-11	Add reference circuit	YES
3	1.2	2019-03-21	Alignment correction	YES
4	1.3	2025-06-09	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

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