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Vinka Microelectronics

VK1620 Datasheet

RAM Mapping 32×4 LCD Controller

Rev.1.1

1 General Description

The VK1620 is a RAM-mapped LCD segment driver capable of supporting up to 128 segments (32 SEG × 4 COM). It supports 2-COM,3-COM and 4-COM display configurations.

The device communication via a 3-wire or 4-wire serial interface,which is used for display parameter configuration, data transmission, and Power-down control.

2 Key Features

- Operating voltage:2.4-3.3V
- LCD voltage: 3.6V to 4.9V
- Low operating current: less than 3μA at 3V
- External crystal input: 32.768 kHz (OSCO, OSCI)
- Selectable LCD bias:1/2 or 1/3
- Selectable LCD duty:1/2, 1/3 or 1/4
- Internal time base frequency source
- Configurable buzzer output: 2 kHz or 4 kHz
- On-chip capacitor type bias charging pump
- Time base or WDT overflow output
- Eight selectable clock sources for time base / WDT
- 32×4LCD driver
- Built-in 32 × 4-bit display RAM
- Three-wire serial interface
- Internal LCD driver frequency source
- Software configuration characteristics
- The read/write addresses increase automatically
- Data mode and command mode instructions
- Three RAM accessing modes
- Available Packages:
  LQFP64（7.0mm × 7.0mm PP=0.4mm）

3 Product Selection

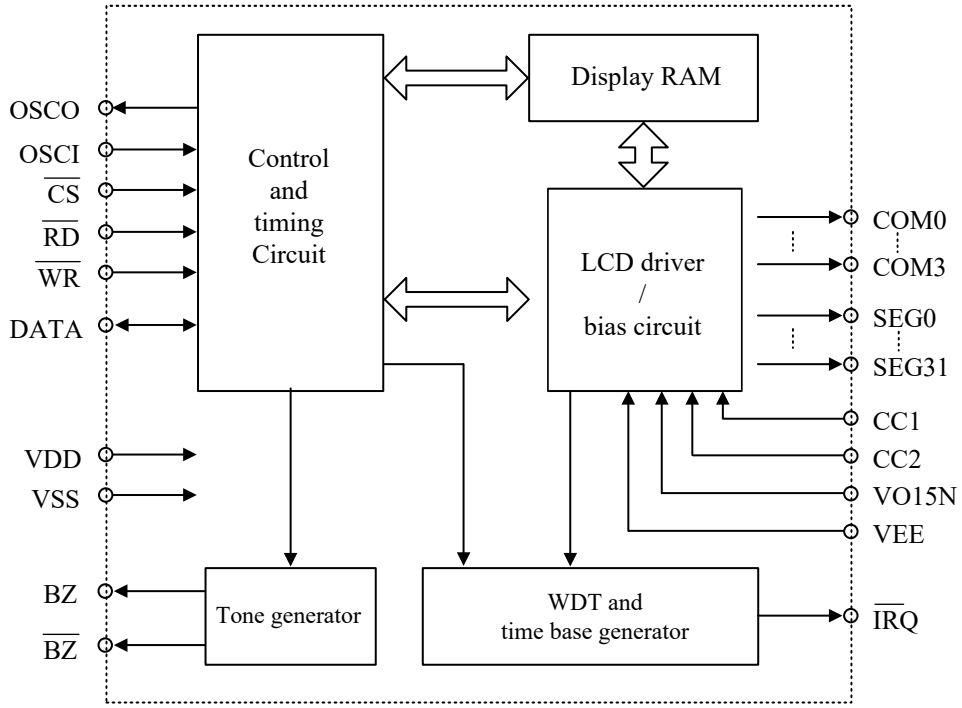
Part No.	VK1620	VK1621S-1	VK1622S-1	VK1623S	VK1625	VK1626
COM	4	4	8	8	8	16
SEG	32	32	32	48	64	48
On-chip Oscillator	-	√	√	√	√	√
Crystal Oscillator	√	√	-	√	√	√
External clock	√	√	√	√	√	√

4 Ordering Information

Part No.	Packaging	Tube Qty	Tray Qty	Box Qty	Total Qty	Notes
VK1620	LQFP64		250/tray	2500/box	15000 PCS	
	DICE		300/tray	1500/box	3000 PCS	DICE
VK1621S-1	LQFP44		160/tray	1600/box	9600 PCS	
	LQFP48		250/tray	2500/box	15000 PCS	
	SSPO48	30/tube		2400/box	24000 PCS	
	DICE		300/tray	1500/box	3000 PCS	DICE
VK1622S-1	LQFP44		160/tray	1600/box	5400 PCS	
	LQFP52		90/tray	900/box	5400 PCS	
	LQFP64		250/tray	2500/box	15000 PCS	
	QFP64		66/tray	660/box	3960 PCS	
	DICE		250/tray	1000/box	2000 PCS	DICE
VK1623S	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		100/tray	500/box	1000 PCS	DICE
VK1625	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		100/tray	500/box	1000 PCS	DICE
VK1626	LQFP100		90/tray	900/box	5400 PCS	
	QFP100		66/tray	660/box	3960 PCS	
	DICE		110/tray	550/box	1500 PCS	DICE

5 Functional Description

5.1 Block Diagram



note： $\overline{CS}$：Chip selection

BZ，$\overline{BZ}$：Sound output

$\overline{WR}$，$\overline{RD}$，DATA：Serial interface

COM0~COM3，SEG0~SEG31：LCD Output

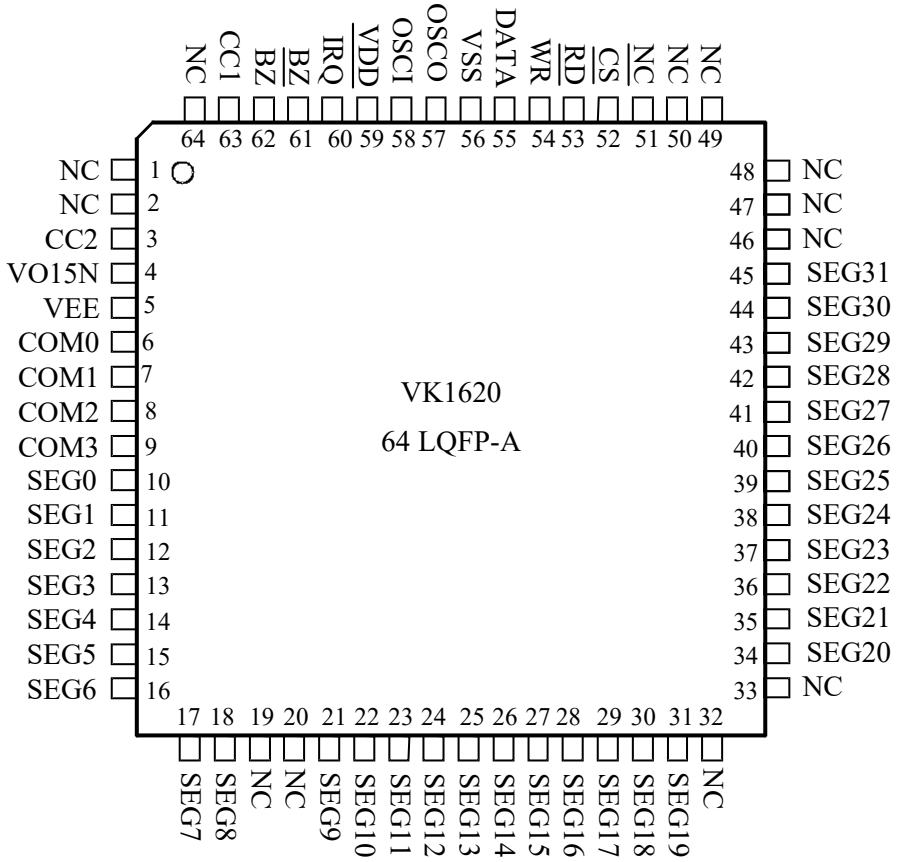
$\overline{IRQ}$：Time base or WDT overflow output

VO15N：Half-voltage circuit output pin

VEE：Output pin of the voltage doubling circuit

CC1/CC2：External capacitor pins, used in voltage doubling and half-voltage circuits

6 Package Pinout Information(LQFP64)



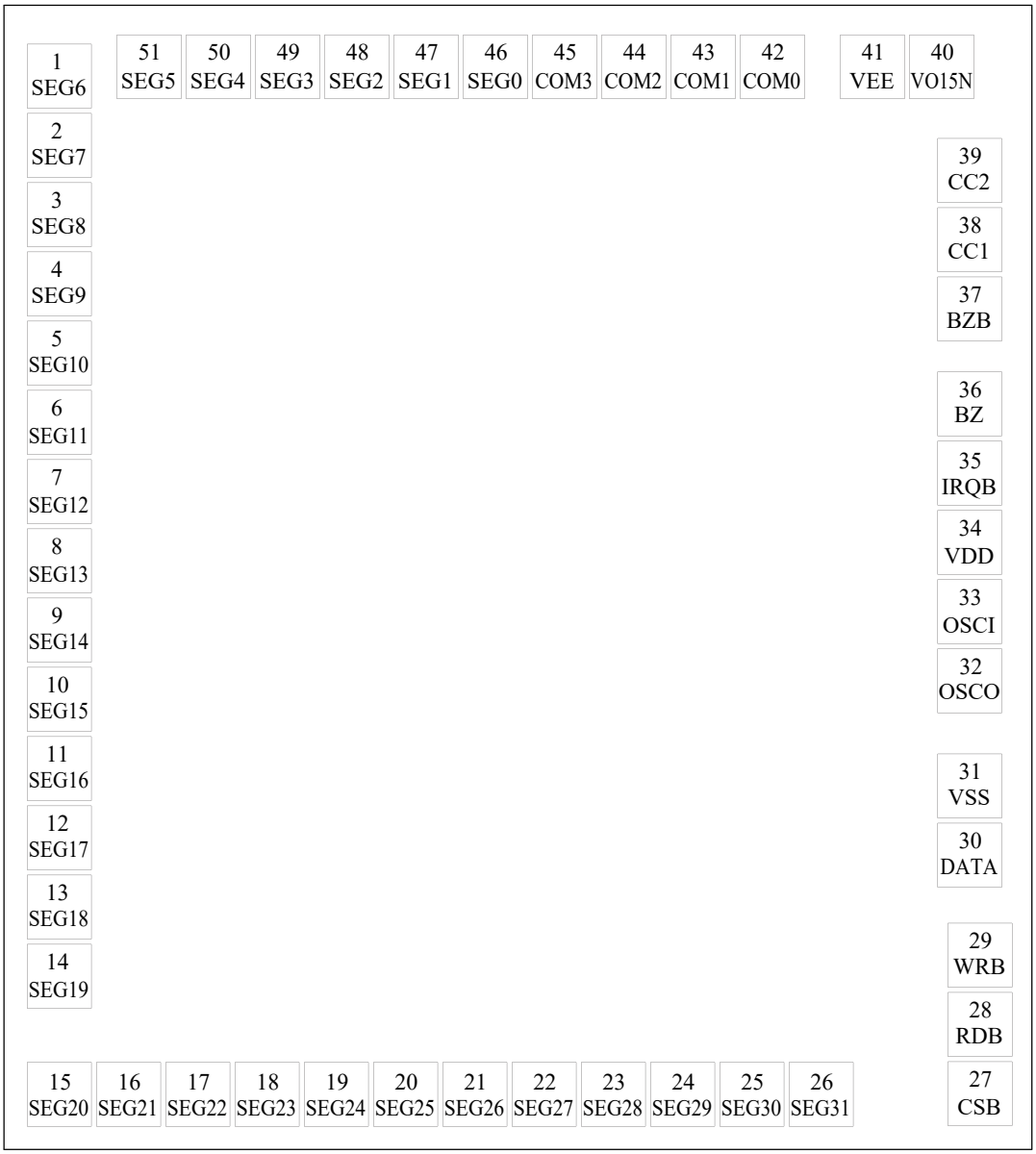
For more information: Page 16

6.1 VK1620/LQFP64 Pin Description

No.	Name	I/O	Function
2	VO15N	O	Half-voltage circuit output pin
3	VEE	—	Output pin of the voltage doubling circuit
4~7	COM0~COM3	O	LCD COM outpu
8~39	SEG0~SEG31	O	LCD SEG outpu
40	$\overline{CS}$	I	Chip selection input with pull-up resistor. When $\overline{CS}$ is at a high level, reading/writing to data and commands of VK1620 is prohibited. The serial port circuit is also in the reset state. If $\overline{CS}$ is at a low level, the read/write function is enabled.
41	$\overline{RD}$	I	A clock reading input with a pull-up resistor. The data of the internal RAM of VK1620 is output at the falling edge of the $\overline{RD}$ signal. The output DATA appears on the Data line. The master controller can lock the data at the next rising edge.
42	$\overline{WR}$	I	Write clock input with pull-up resistor. The DATA on the data line is in the $\overline{WR}$ signal. The rising edge is locked to VK1620.
43	DATA	I/O	Serial data input/output with pull-up resistor
44	VSS	—	VSS
45	OSCO	O	OSCI and OSCO are connected to a 32.768kHz crystal oscillator to generate the system clock.
46	OSCI	I	
47	VDD	—	VDD
48	$\overline{IRQ}$	O	Time base or WDT overflow flag,NMOS open-drain output
49, 50	BZ, $\overline{BZ}$	O	2kHz or 4kHz pitch frequency output (three-state output buffer)
51, 1	CC1, CC2	I	External capacitor pins for use in voltage doubling circuits and half-voltage circuits.

7 COB Pad Information

7.1 COB Pad Assignment



Chip Dimensions: 1650×1750 μm ², Substrate potential: VDD,
Pad size: 90×85 μm,

7.2 COB PAD Coordinates

Unit: um

Pad No	Name	X	Y	Pad No	Name	X	Y
1	SEG6	-740.300	780.050	27	CSB	706.550	-793.550
2	SEG7	-740.300	670.050	28	RDB	706.550	-683.550
3	SEG8	-740.300	560.050	29	WRB	706.550	-573.550
4	SEG9	-740.300	450.050	30	DATA	689.700	-445.450
5	SEG10	-740.300	340.050	31	VSS	689.700	-334.300
6	SEG11	-740.300	230.050	32	OSCO	689.700	-187.150
7	SEG12	-740.300	120.050	33	OSCI	689.700	-77.150
8	SEG13	-740.300	10.050	34	VDD	689.700	34.850
9	SEG14	-740.300	-99.950	35	IRQB	689.700	146.850
10	SEG15	-740.300	-209.950	36	BZ	689.700	256.850
11	SEG16	-740.300	-319.950	37	BZB	689.700	455.750
12	SEG17	-740.300	-429950	38	CC1	689.700	565.750
13	SEG18	-740.300	-539.950	39	CC2	689.700	675.750
14	SEG19	-740.300	-649.950	40	VO15N	640.700	789.950
15	SEG20	-744.300	-789.950	41	VEE	530.700	789.950
16	SEG21	-634.300	-789.950	42	COM0	394.700	789.950
17	SEG22	-524.300	-789.950	43	COM1	284.700	789.950
18	SEG23	-414.300	-789.950	44	COM2	174.700	789.950
19	SEG24	-304.300	-789.950	45	COM3	64.700	789.950
20	SEG25	-194.300	-789.950	46	SEG0	-45.300	789.950
21	SEG26	-83.300	-789.950	47	SEG1	-155.300	789.950
22	SEG27	25.700	-789.950	48	SEG2	-265.300	789.950
23	SEG28	135.700	-789.950	49	SEG3	-375.300	789.950
24	SEG29	245.700	-789.950	50	SEG4	-485.300	789.950
25	SEG30	355.700	-789.950	51	SEG5	-595.300	789.950
26	SEG31	465.700	-789.950				

8 Limit Parameters

Power supply voltage ..... -0.3V~3.6V

Input voltage ..... V_{SS}-0.3V~V_{DD}+0.3V

Storage temperature ..... -50℃~125℃

Working temperature ..... -45℃~85℃

8.1 DC Electrical Characteristics

Ta=25℃

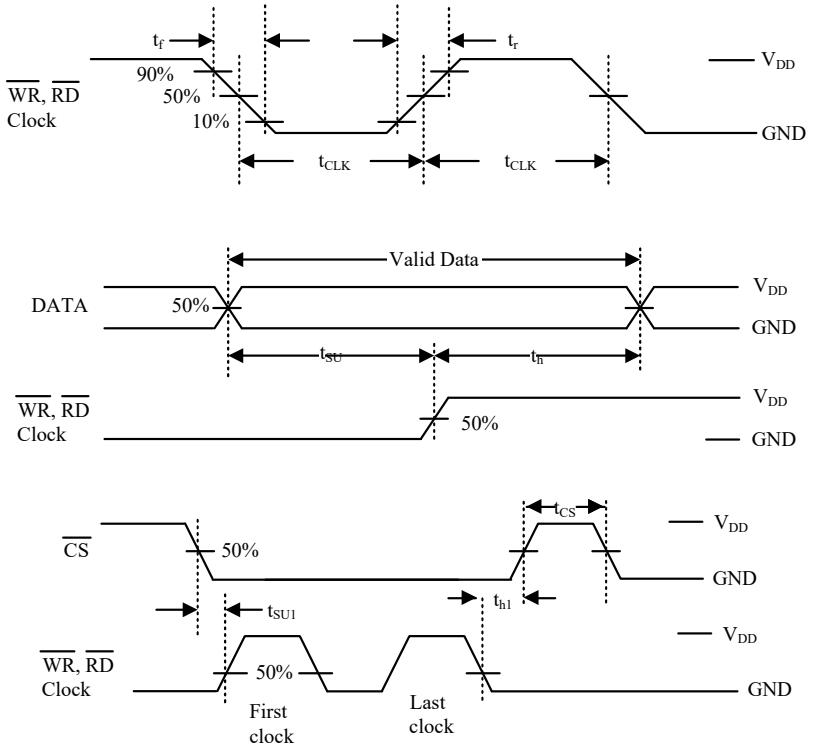
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
V_{DD}	Working voltage	—	—	2.4	—	3.3	V
I_{DD}	Working current	3V	No load*1	—	2	3	uA
I_{STB}	Standby current	3V	No load*2	—	1	5	uA
V_{IL}	Low-level input voltage	3V	DATA,$\overline{WR}$,$\overline{CS}$,$\overline{RD}$	—	—	1	V
V_{IH}	High-level input voltage	3V	DATA,$\overline{WR}$,$\overline{CS}$,$\overline{RD}$	2.4	—	3.0	V
I_{OL1}	DATA,BZ,$\overline{BZ}$,IRQ	3V	V_{OL}=0.3V	0.8	1.6	—	mA
I_{OH1}	DATA,BZ,$\overline{BZ}$	3V	V_{OH}=2.7V	-0.6	-1.2	—	mA
I_{OL2}	LCD COM Sink Current	3V	V_{OL}=0.3V	80	150	—	uA
I_{OH2}	LCD COM Source Current	3V	V_{OH}=2.7V	-70	-120	—	uA
I_{OL3}	LCD SEG Sink Current	3V	V_{OL}=0.3V	70	140	—	uA
I_{OH3}	LCD SEG Source Current	3V	V_{OH}=2.7V	-30	-60	—	uA
R_{PH}	Pull-UP Resistor	3V	DATA,$\overline{WR}$,$\overline{CS}$,$\overline{RD}$	40	80	150	kΩ

*1 No-load :LCD on, buzzer off，$\overline{CS}$=$\overline{WR}$=$\overline{RD}$= high level
*2 No-load :LCD off, buzzer off，$\overline{CS}$=$\overline{WR}$=$\overline{RD}$= high level

8.2 AC Electrical Characteristics

Ta=25℃

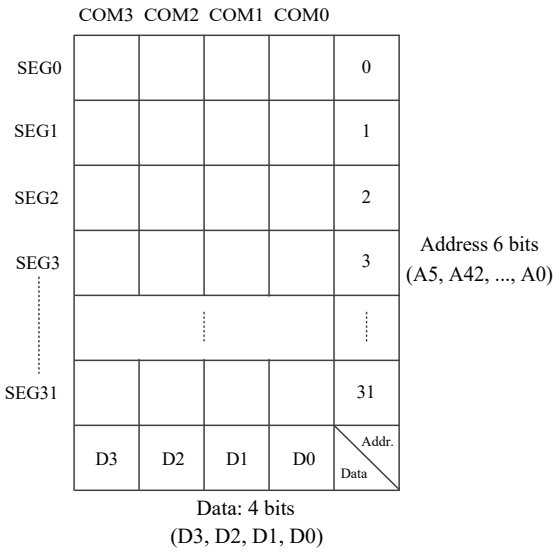
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
f_{SYS}	System clock	3V	On-chip RC oscillator	—	256	—	kHz
f_{LCD}	LCD clock	—	32kHz crystal oscillator	—	64	—	Hz
		—			64	—	Hz
		—		—	56	—	Hz
		—		—	64	—	Hz
t_{COM}	LCD Common Period	—	N:Number of COM	—	n/f_{LCD}	—	s
f_{CLK}	Serial Data Clock ($\overline{WR}$)	3V	Write mode	—	—	150	kHz
			Read mode	—	—	75	kHz
f_{TONE}	Pitch frequency	—	—	—	2 or 4	—	kHz
t_{CS}	Serial Interface Reset PW	—	$\overline{CS}$	—	250	—	ns
t_{CLK}	$\overline{WR}$, $\overline{RD}$ Input pulse width	3V	Write mode	3.34	—	—	us
			Read mode	6.67	—	—	
t_r ,t_f	Rise/Fall Time Serial Data Clock Width	3V	—	—	120	—	ns
t_{su}	Setup Time for DATA to /$\overline{WR}$, /$\overline{RD}$ Clock Width	3V	—	—	120	—	ns
t_h	Hold Time for DATA to /$\overline{WR}$, /$\overline{RD}$ Clock Width	3V	—	—	120	—	ns
t_{su1}	Setup Time for /$\overline{CS}$ to /$\overline{WR}$, /$\overline{RD}$ Clock Widt	3V	—	—	100	—	ns
t_{h1}	Hold Time for /$\overline{CS}$ to /$\overline{WR}$, /$\overline{RD}$ Clock Width	3V	—	—	100	—	ns



9 Function Description

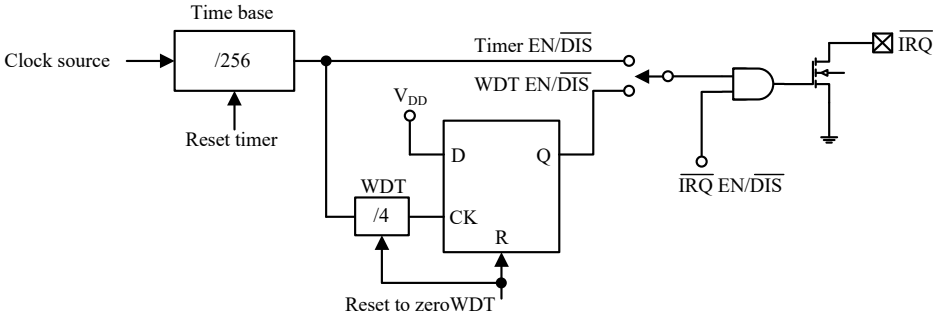
9.1 Display Memory Area -RAM structure

The static display storage area (RAM) of VK1620 is 32×4 bits, which is used to store display data. The content of RAM is directly mapped to the content of the LCD driver. The data in RAM can be accessed using the READ, WRITE and read-modifiy-write commands. The following is the mapping diagram of RAM.



9.2 Time Base and WDT

The time base generator and WDT share an 8-bit (/256) counter. The DIS/ ENCLR of the timer, the DIS/ EN/ CLR of the WDT and the EN/ DIS of the IRQ are independent of each other. Once the WDT times out, the IRQ pin will remain low until the CLRWDT or IRQDIS command is executed.



Timer and WDT configuration

9.3 Tone Output

The VK1620 is equipped with a simple tone generator inside, which can output a pair of differential-driven signals from BZ and /BZ to generate a single tone.

9.4 LCD Driver

The VK1620 is a 128(32×4) dot LCD driver. It can be configured through software to be 1/2 or 1/3 biased, with 2, 3 or 4 COM outputs. This feature makes the VK1620 suitable for various LCD applications. The LCD driver clock is provided by the system clock. The frequency of the driving clock is 256KHz. The relevant commands are shown in the table below. The 100 in bold format, namely 100, represents the command mode ID. If consecutive commands are executed, the ids of all command patterns except the first one will be omitted. The LCD OFF command turns off the LCD display by disabling the LCD bias generator. In contrast, the LCD ON command turns on the LCD display by enabling the LCD bias generator. Both "BIAS" and "COM" are commands related to LCD displays. By using these commands, VK1620 can be compatible with most types of LCD displays

Name	Command code	Function
LCD OFF	**100**00000010X	Turn off the LCD output
LCD ON	**100**00000011X	Turn on the LCD output
BIAS and COM	**100**0010abXcX	c= 0:1/2 bias option c= 1:1/3 bias option ab= 00:2 COM option ab= 01:3 COM option ab= 10:4 COM options

9.5 Command Format

The VK1620 can be configured through software Settings. There are two mode commands for configuring the VK1620 and transmitting LCD display data. The configuration mode of VK1620 is also called the command mode, and its command mode ID is 100. The command mode includes system configuration commands, system frequency selection commands, LCD configuration commands, tone frequency selection commands, timer /WDT setting commands and operation commands, while the data mode includes read, write and read - modify - write operations. The following table lists the command mode ids and data mode ids.

Command	Mode	ID
READ	Data	110
WRITE	Data	101
READ-MODIFY-WRITE	Data	101
COMMAND	Command	100

Mode commands should be executed before sending data or commands. If consecutive commands are executed, command pattern D can be omitted. When the system executes discontinuous commands or discontinuous address data modes, the CS pin should be set to a high level, and the previous operation mode will be reset simultaneously. When the CS pin returns to low power, the new operation mode ID should be executed first.

9.6 Interface

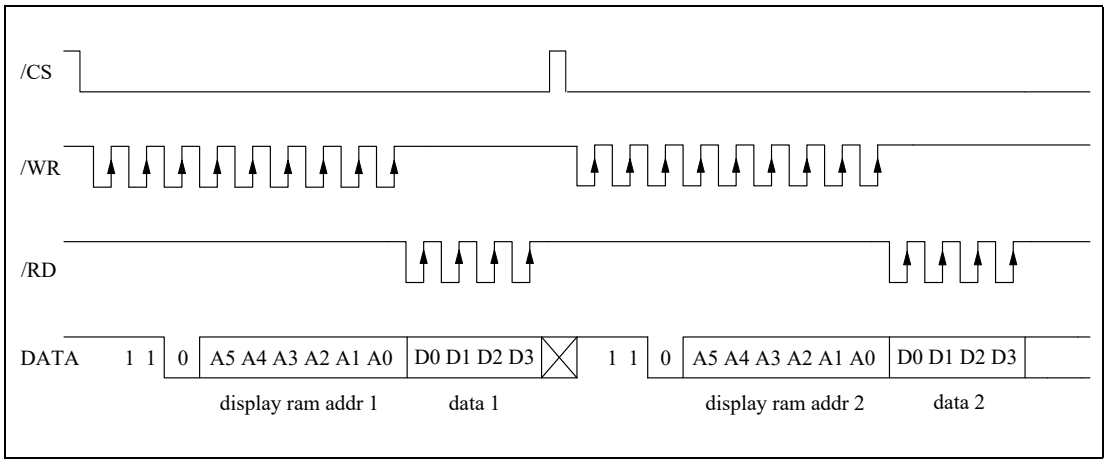
Only four wires are needed for the VK1620 interface. The CS line is used to initialize the serial interface circuit and terminate the communication between the master controller and the VK1620. If the CS pin is set to 1, the communication between the master controller VK1620 is first prohibited and then initialized. When executing mode commands or performing mode switching, a high-level pulse is required to initialize the serial interface of the VK1620. The DATA line is a serial data input/ output line. The DATA read and written as well as the commands executed must all pass through the data line. The RD line is the clock reading input. The DATA in RAM is output at the falling edge of RD, and the output data will appear on the Data line. The master controller should read the correct data between the rising edge and the next falling edge of the RD signal. The WR line is the input for writing the clock. The DATA, addresses and commands on the Data line are all input VK1620 at the rising edge of the WR signal. In addition, there is an optional IRQ cable that can be connected to the controller and VK1620. The IRQ pin can be set by software as a timer output or a WDT overflow flag output.

10 Cmd/Data Timing Diagram

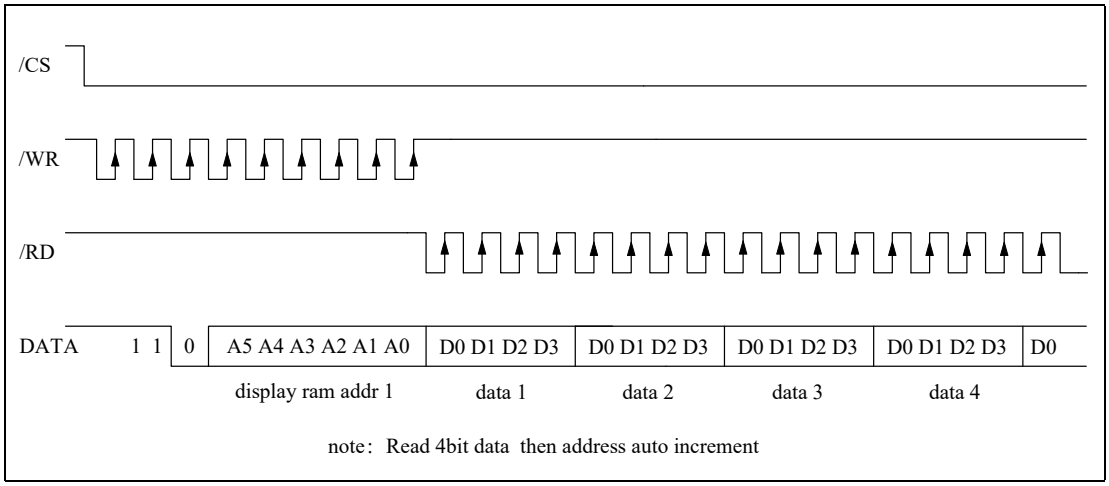
The following are the data mode IDs and the command mode ID Timing Diagrams.

10.1 READ Mode

Command Code : 110

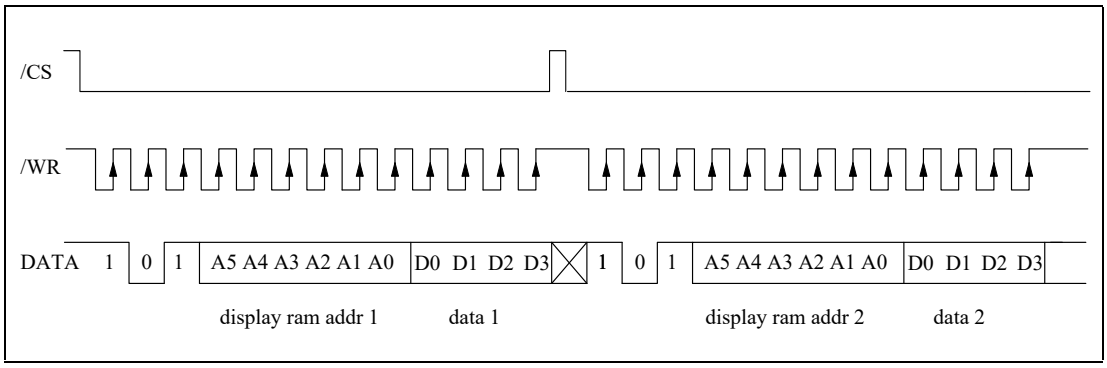


Successive Address Reading

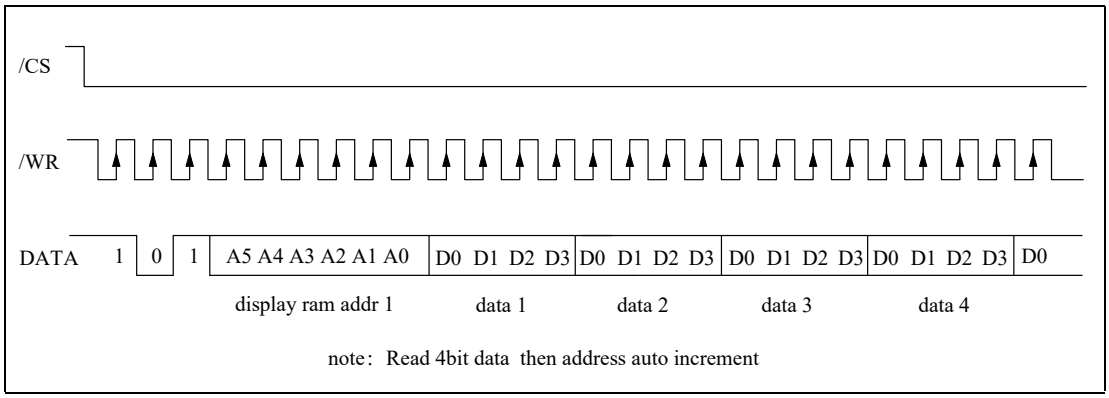


10.2 WRITE Mode

Command Code : 101

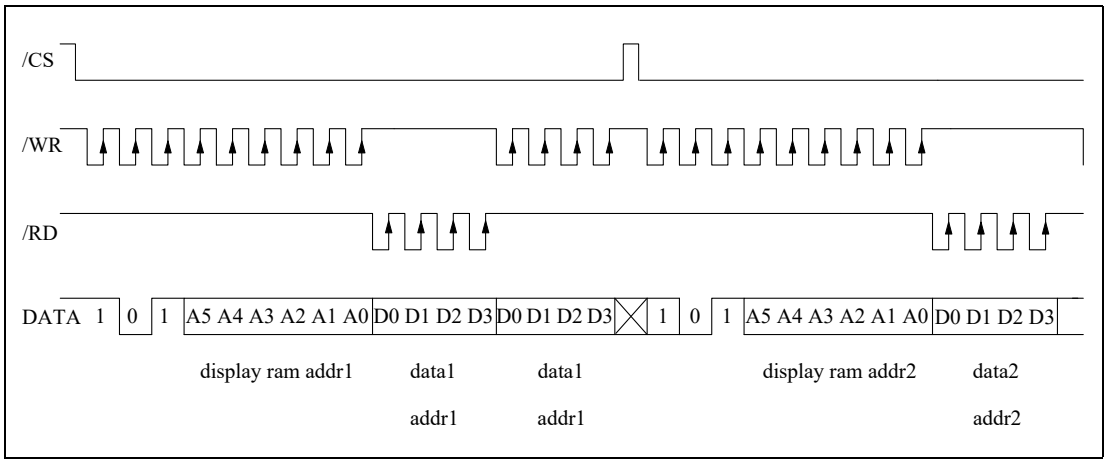


Successive Address Writing

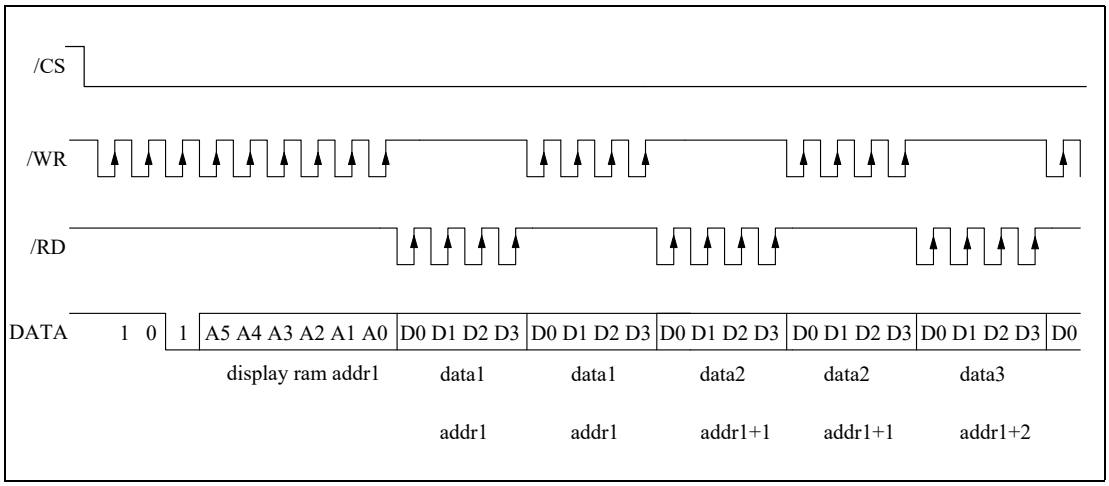


10.3 Read-Modify-Write Mode

Command Code : 101

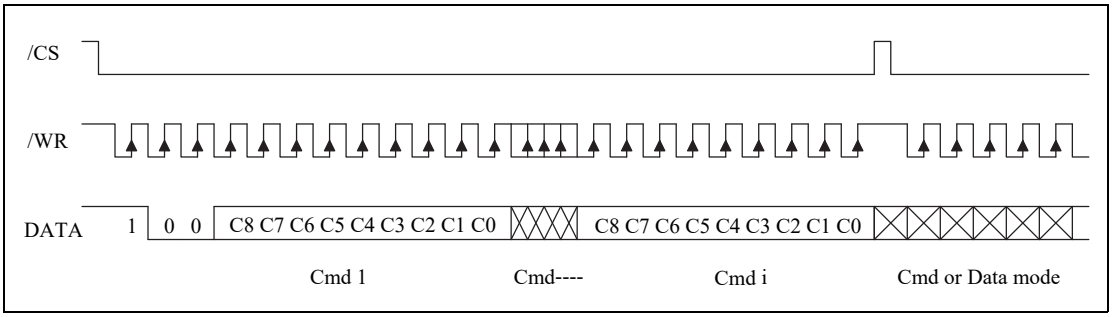


Successive Address Accessing



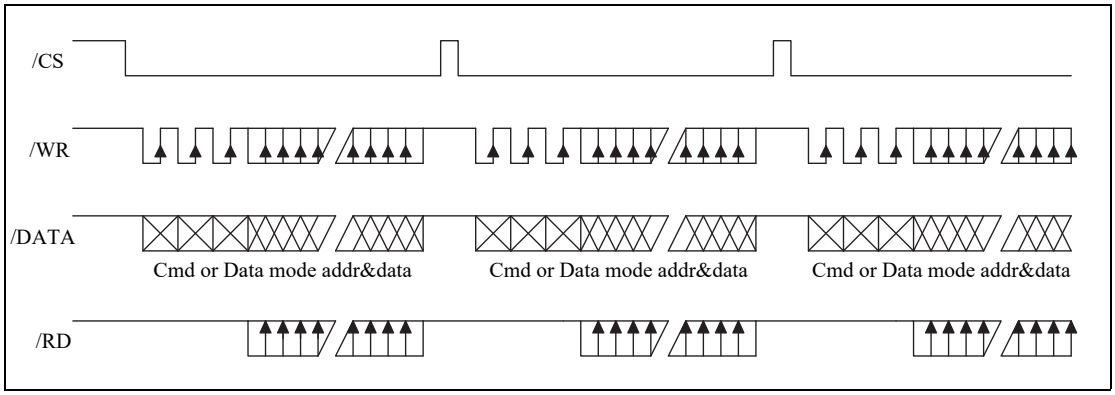
10.4 Command Mode

Command Code : 100



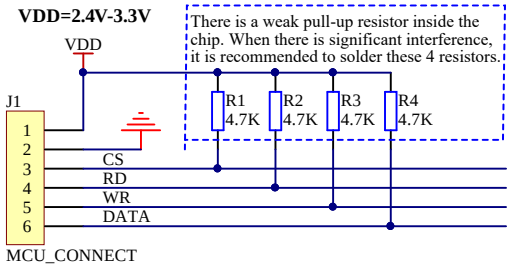
10.5 Data and Command Mode

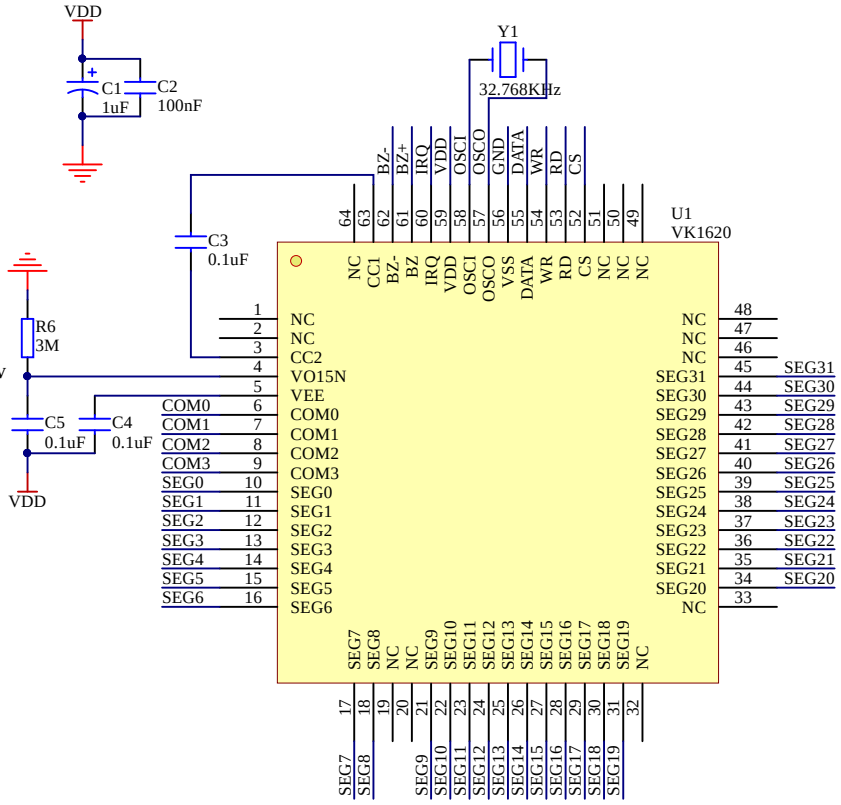
Data and Command Mode



11 Application Circuits

LCD only requires the RD pin to be left floating and not connected.
When there is significant external interference, a 10R to 1k resistor and a pF-level capacitor connected to ground can be connected in series on the communication pins.

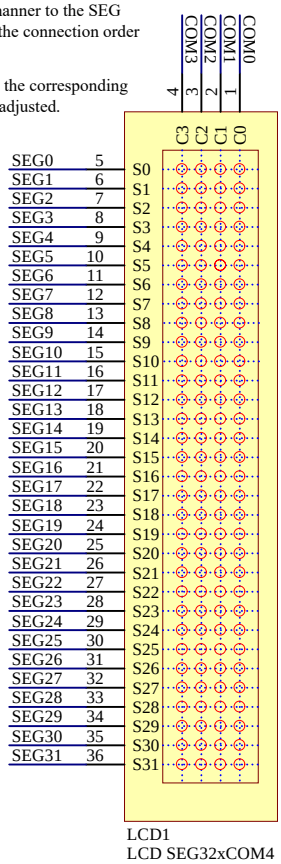


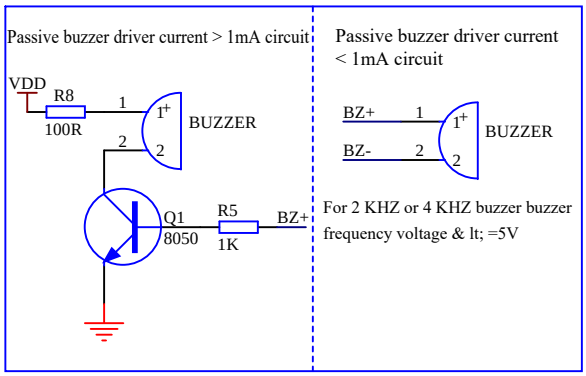


For **1/2 Bias, VDD =2.4V~3.3V, VEE =0V, VicD (LCD** Voltage)= **VpD-VEE=2.4V~3.3V**
For **1/3 Bias, Vop =2.4V~3.3V, VEE =-1/2 Vpp, VicD (LCD Voltage)= Voo-VEE =3/2 Vop =3.6V~4.9V**

It is recommended that the COM pins of the chip and the COM pins of the LCD be connected in a 1-to-1 manner to the SEG pins. For the convenience of PCB routing, the connection order can be changed.

Please note that when writing the software, the corresponding order of the display RAM also needs to be adjusted.





12 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY -WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off system oscillator	Yes
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	Yes
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
TIMER DIS	100	0000-0100-X	C	Disable time base output	Yes
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag outpu	Yes
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	Yes
TONE ON	100	0000-1001-X	C	Turn on tone outputs	
CLR TIMER	100	0000-1101-X	C	Clear the contents of time base generator	
CLR WDT	100	0000-111X-X	C	Clear the contents of WDT stage	
BIAS 1/2	100	0010-abX0-X	C	LCD 1/2 bias option ab=00：2 COM ab=01：3 COM ab=10：4 COM	
BIAS 1/3	100	0010-abX1-X	C	LCD 1/3 bias option ab=00：2 COM ab=01：3 COM ab=10：4 COM	
TONE 4K	100	010X-XXXX-X	C	Tone frequency, 4kHz	
TONE 2K	100	011X-XXXX-X	C	Tone frequency, 2kHz	
$\overline{\text{IRQ}}$ DIS	100	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	Yes
$\overline{\text{IRQ}}$ EN	100	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	100	101X-0000-X	C	Time base/WDT clock output:1Hz The WDT time-out flag after: 4s	
F2	100	101X-0001-X	C	Time base/WDT clock output:2Hz The WDT time-out flag after: 2s	
F4	100	101X-0010-X	C	Time base/WDT clock output:4Hz The WDT time-out flag after: 1s	

F8	100	101X-0011-X	C	Time base/WDT clock output:8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-0100-X	C	Time base/WDT clock output:16Hz The WDT time-out flag after: 1/4s	
F32	100	101X-0101-X	C	Time base/WDT clock output:32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-0110-X	C	Time base/WDT clock output:64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-0111-X	C	Time base/WDT clock output:128Hz The WDT time-out flag after: 1/32s	Yes
TEST	100	1110-0000-X	C	Test mode	
NORMAL	100	1110-0011-X	C	Normal mode	Yes

Note: X: Irrelevant position

A5 to A0: RAM address

D3 to D0: RAM data

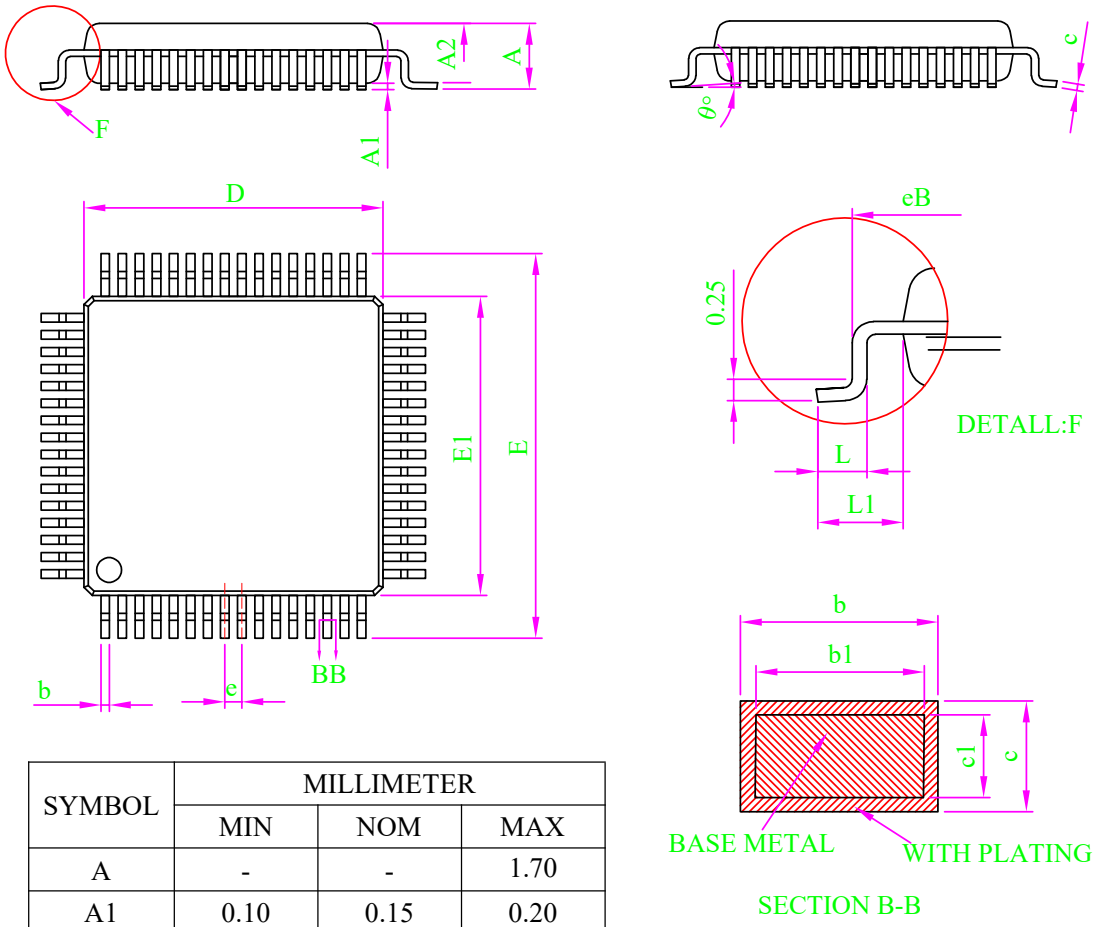
D/C: Data/Command Mode

Def: Default reset upon power-on

All the bold 110,101 and 100 are pattern commands. Among them, 100 represents the command pattern ID. If consecutive commands are executed, the command pattern ids after the first command are all ignored. The pitch frequency and the clock of the time base /WDT can be driven by a 32.768KHz crystal oscillator. Since power-on reset may fail, it is recommended to initialize the VK1620 using the master controller after power-on reset.

13 Package Information

13.1 LQFP64（7.0mm × 7.0mm PP=0.4mm）



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.70
A1	0.10	0.15	0.20
A2	1.30	1.40	1.50
b	0.16	-	0.24
b1	0.15	0.18	0.21
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-	8.28
e	0.40 BSC		
L	0.42	0.57	0.72
L1	0.95	1.00	1.15
θ	0	-	10°

Note:

1. All dimension are in mm.
2. Dim D&El does not include plastic flash； Flash: Plastic residual around body edge after de junk/singulation.
3. Dim b does not include dambar protrusion/intrusion.
4. Plating thickness 0.007mm-0.015mm

14 Disclaimer

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15 Revision History

No.	Version	Date	Modify the content	Check
1	1.0	2022-08-09	initial release	YES
2	1.1	2025-07-09	Change Description	YES

[1] Please refer to the latest version of this document before starting or finalizing any design.

[2] Since the release of this document, the status or availability of this product may have changed. For the most up-to-date information, please visit: https://www.szvinka.com/